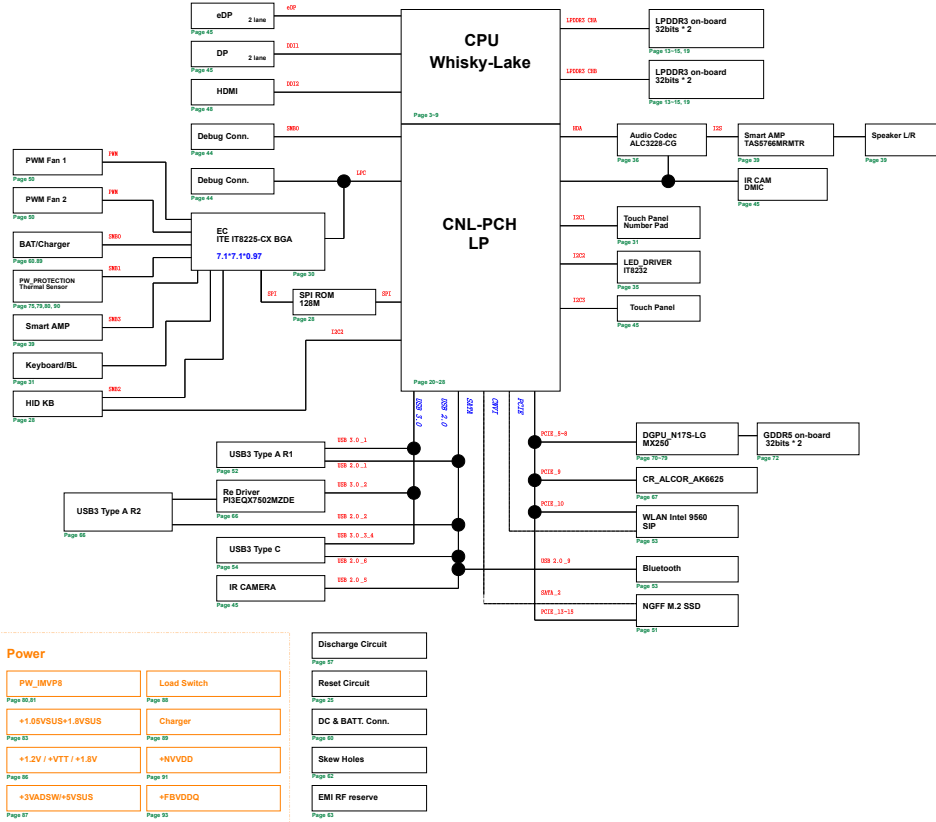


PAGE	Content
1	Block Diagram
2	System Setting
3	CPU_DISPLAY
4	CPU_LPDDR3
5	CPU_LFC,SPI,SMB,CLINK
6	CPU_POWER
7	
8	CPU_MISC,JTAG,CLK
9	CPU_CFG,RSTVD
10	CPU_POWER_CAP
11	
13	LPDDR3 TERMINATION
14	LPDDR3_ON-BOARD_A
15	LPDDR3_ON-BOARD_B
19	LPDDR3_CA_DQ VOLTAGE
20	CPU_FCH_CS12,BMMC,CNV
21	CPU_FCH_OSDIO, LPDIO, MISC
22	CPU_FCH_AUDIO,SDIO,SDXC
23	CPU_FCH_PCIE,USB,SATA
24	CPU_FCH_CLOCK SIGNALS,RTC
25	CPU_FCH_VTV_POWER
26	CPU_FCH_POWER,GND
27	CPU_FCH_POWER,GND
28	FCH-SPI ROM,OTH
29	
30	WBC_I78225
31	EC_KB_TP
34	
35	LED_DRIVER_I78232
36	AUD-ALC1288
38	AUD_Headphone
39	AUD_SMA_TSA576GM
44	BUG_Debug
45	LCD_Panel_CMOS_CMIC
46	IR_CMIC BD
48	HDMI-type D
50	FAN & CPU Thermal Sensor
51	NGFF(KEY-M)_SSD
52	USB 3.0_Type_A_R1
53	WLAN_SIP_PCIE_CNVI
54	USB 3.0_Type_C
56	LED Indicator
57	DWG_Discharge
58	FRO_Protect
60	PW_DC JACK / BAT CON
62	MC Conn & Skew Role
63	EMI_RF Reserve
66	USB 3.0_Type_A_R2
67	Micro SD_ALCOR_AK6625
70	GPU_PCIE-EXPRESS
71	GPU_MEMORY INTERFACE-A
72	FRAME_BUFFER****
74	GPU_STRAPPING/XTAL
75	GPU_GPIO_THERM
76	GPU_VDD/GND
77	GPU_PWG DISCOUPLING
78	GPU Power
79	VGA_sensor
80	PW_CHL_MPS2979 (1)
81	PW_CHL_MPS2979 (2)
83	PW_+1.05VSUS/+1.8VSUS
86	PW_+1.2V/VTT
87	PW_+3VADSW/+5VSUS
88	PW_LOAD SWITCH
89	PW_CHARGER
90	PW_PROTECTION
91	PW_+BVDD (I78820 2PH)
93	PW_+FBVDDQ

UX481FL Series SCHEMATIC Revision 2.0

Connected Standby



[illegible]

Name	Crating	Signal Name	Default	IO	Set bit on (min)	Power
00000	0	1000_0000	1000	00	1000 0000	
00001	0	1000_0001	1000	00	1000 0001	
00002	0	1000_0010	1000	00	1000 0010	
00003	0	1000_0011	1000	00	1000 0011	
00004	0	1000_0100	1000	00	1000 0100	
00005	0	1000_0101	1000	00	1000 0101	
00006	0	1000_0110	1000	00	1000 0110	
00007	0	1000_0111	1000	00	1000 0111	
00008	0	1000_1000	1000	00	1000 1000	
00009	0	1000_1001	1000	00	1000 1001	
00010	0	1000_1010	1000	00	1000 1010	
00011	0	1000_1011	1000	00	1000 1011	
00012	0	1000_1100	1000	00	1000 1100	
00013	0	1000_1101	1000	00	1000 1101	
00014	0	1000_1110	1000	00	1000 1110	
00015	0	1000_1111	1000	00	1000 1111	
00016	0	1001_0000	1001	00	1001 0000	
00017	0	1001_0001	1001	00	1001 0001	
00018	0	1001_0010	1001	00	1001 0010	
00019	0	1001_0011	1001	00	1001 0011	
00020	0	1001_0100	1001	00	1001 0100	
00021	0	1001_0101	1001	00	1001 0101	
00022	0	1001_0110	1001	00	1001 0110	
00023	0	1001_0111	1001	00	1001 0111	
00024	0	1001_1000	1001	00	1001 1000	
00025	0	1001_1001	1001	00	1001 1001	
00026	0	1001_1010	1001	00	1001 1010	
00027	0	1001_1011	1001	00	1001 1011	
00028	0	1001_1100	1001	00	1001 1100	
00029	0	1001_1101	1001	00	1001 1101	
00030	0	1001_1110	1001	00	1001 1110	
00031	0	1001_1111	1001	00	1001 1111	
00032	0	1010_0000	1010	00	1010 0000	
00033	0	1010_0001	1010	00	1010 0001	
00034	0	1010_0010	1010	00	1010 0010	
00035	0	1010_0011	1010	00	1010 0011	
00036	0	1010_0100	1010	00	1010 0100	
00037	0	1010_0101	1010	00	1010 0101	
00038	0	1010_0110	1010	00	1010 0110	
00039	0	1010_0111	1010	00	1010 0111	
00040	0	1010_1000	1010	00	1010 1000	
00041	0	1010_1001	1010	00	1010 1001	
00042	0	1010_1010	1010	00	1010 1010	
00043	0	1010_1011	1010	00	1010 1011	
00044	0	1010_1100	1010	00	1010 1100	
00045	0	1010_1101	1010	00	1010 1101	
00046	0	1010_1110	1010	00	1010 1110	
00047	0	1010_1111	1010	00	1010 1111	
00048	0	1011_0000	1011	00	1011 0000	
00049	0	1011_0001	1011	00	1011 0001	
00050	0	1011_0010	1011	00	1011 0010	
00051	0	1011_0011	1011	00	1011 0011	
00052	0	1011_0100	1011	00	1011 0100	
00053	0	1011_0101	1011	00	1011 0101	
00054	0	1011_0110	1011	00	1011 0110	
00055	0	1011_0111	1011	00	1011 0111	
00056	0	1011_1000	1011	00	1011 1000	
00057	0	1011_1001	10			

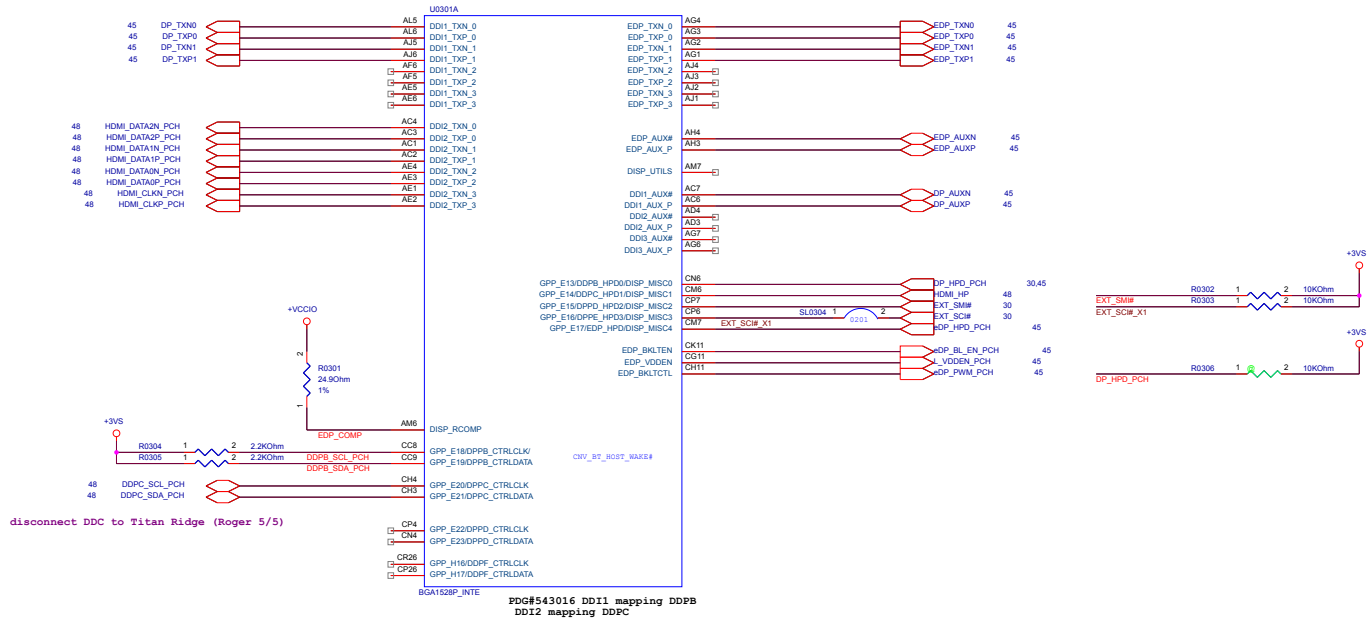
[illegible]

Display Port

A	EDP, First Panel
B	DP, Second Panel
C	HDMI

Intel Version	ASUS P/N
ES-0	01001-01540000

HDMI	
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK



PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPB

LPDDR3 Non-Interleaved

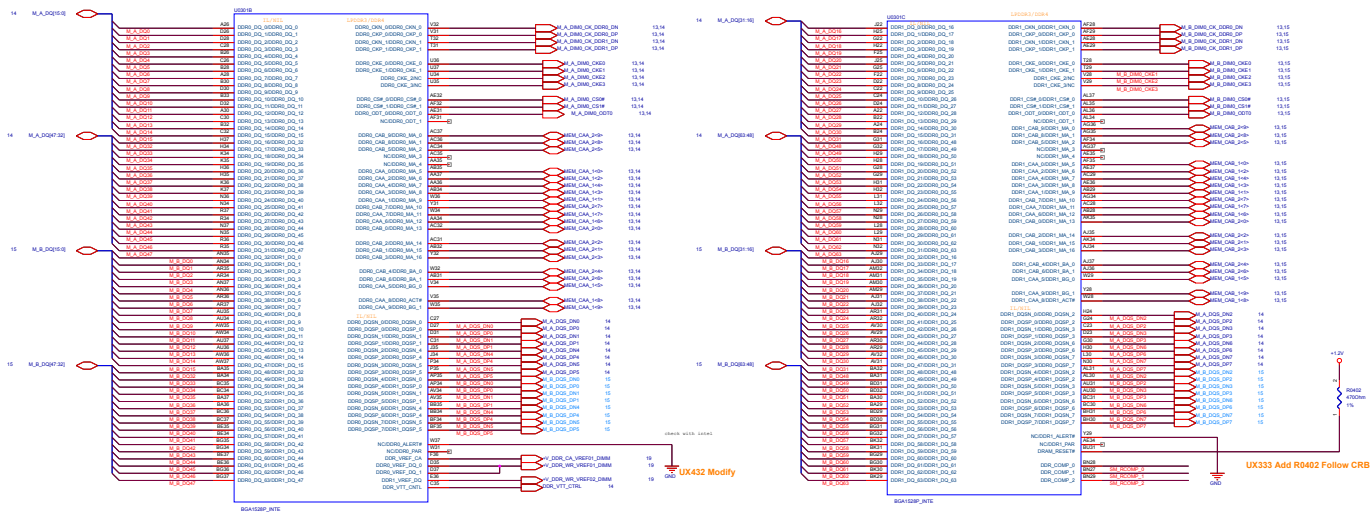
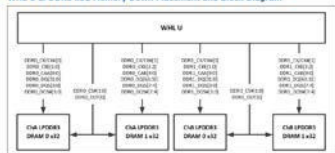
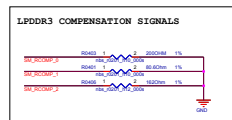


Figure 2-2. WHL U LPDDR3 x32 Memory Down Placement and Block Diagram



RCOMP[0]	M	SL/PL	VSS	5	12-15				20	25		500	500	200
RCOMP[1]	M	SL/PL	VSS	5	12-15				20	25		500	500	80.6
RCOMP[2]	M	SL/PL	VSS	5	12-15				20	25		500	500	142



```
2nd source:
200 chan >>100211200017020(YAGRO), 10101-00001000(TX
162 chan>>10101-00031000(TX-Y), 10101-00031000(YAGRO)
```

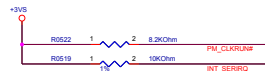
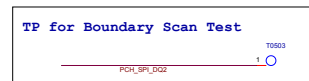
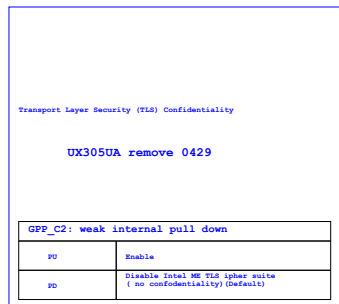
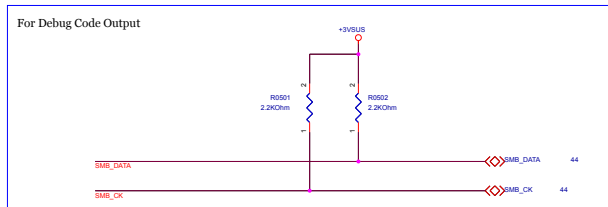
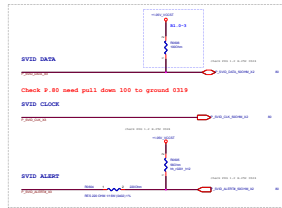


Diagram illustrating the connection of the +3V3V5 pin to various components on the R1.1-5 board:

- +3V3V5 is connected to a network of resistors and capacitors.
- Resistors shown: R0508 (100KOhm), R0503 (2.2KOhm), R0504 (2.2KOhm), R0505 (2.2KOhm), R0506 (2.2KOhm), and R0507 (100KOhm).
- Capacitors shown: 100nF, 100pF, and 1000pF.
- Connections to pins: SMLT_ALERT#, SMLT_CK, SMLT_DATA, SMLD_CK, and SMLD_DATA.



C0672 C0615 C0623 close to CPU 1203



	1995
Living conditions	79
Living together	47
Living alone	790
Living alone	31
Living alone	18
Living alone	5.1
Living alone	8
Living alone	10.9
Living alone	31
Living alone	75

[illegible][illegible]

CAP above 10uF move to PWR page

+=VCGST OnCap
CPU Bank 0-3
Q201 1uF/5.1V X5R 104 *B

10V

10uF/10V X5R 104 *B

1uF/5.1V X5R 104 *B

1uF/5.1V X5R 104 *B

1uF/5.1V X5R 104 *B

1uF/5.1V X5R 104 *B

GND

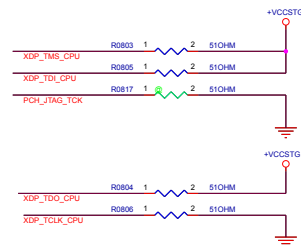
[illegible]

STM32F103C8T6

Pinout diagram of the STM32F103C8T6 microcontroller. The diagram shows the 48 pins of the package, including power pins (VDD, GND), I/O pins (GPIO, I2C, SPI, UART), and other functional pins (JTAG, SWD, etc.). The pins are color-coded: red for power, green for I/O, and blue for other functions. The diagram is labeled 'STM32F103C8T6' at the bottom.

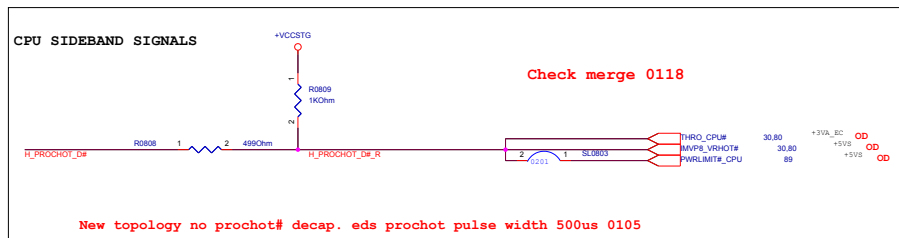
```

DEK32 Del +VCC_EORAM_EOR3D
DEK32 DEL -VCC_EORAM_I2R
  
```



XDP_TDO_CPU	1	T0808
XDP_TMS_CPU	1	T0809
XDP_TRST_CPU#	1	T0810
XDP_TDI_CPU	1	T0802
XDP_TCLK_CPU	1	T0812
PCH_JTAG_TCK	1	T0815

No OPC Check remove 且R0811 R0810量測兩端為0V 0126



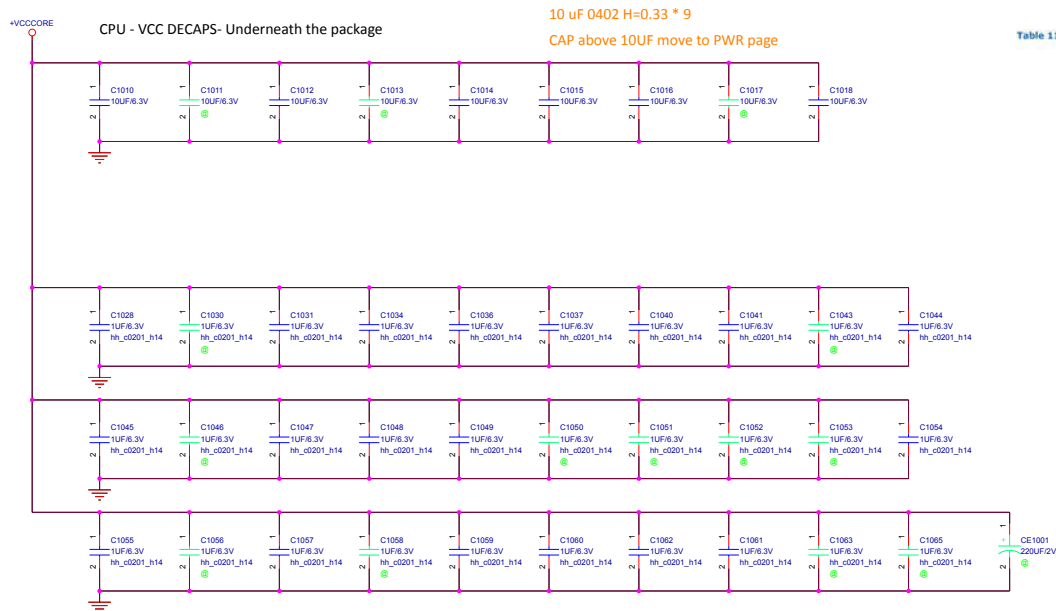
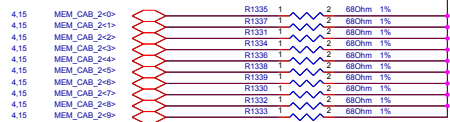
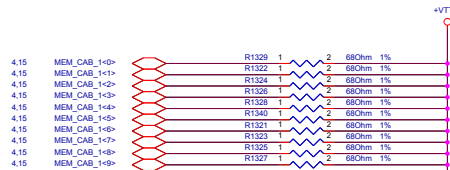
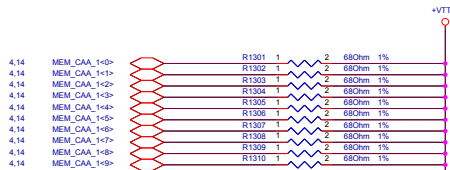


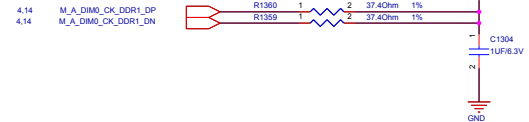
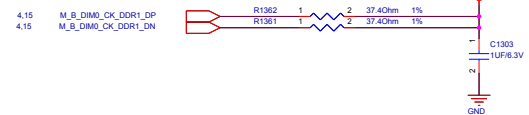
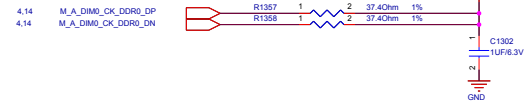
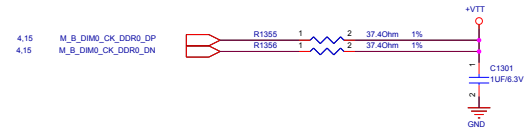
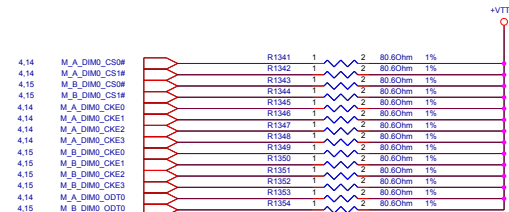
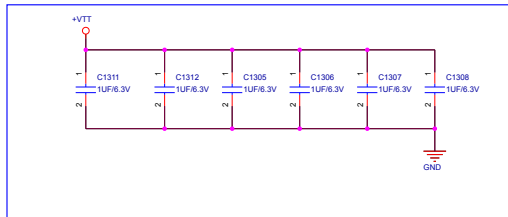
Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCC ₀₉		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
VIO ₀₂	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

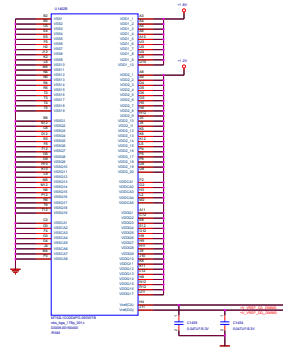
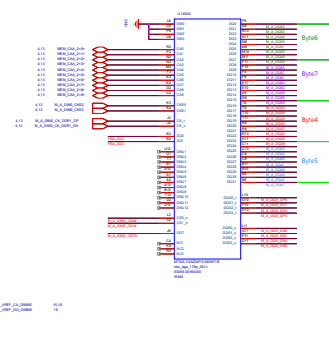
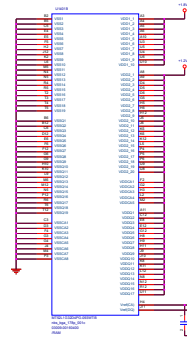
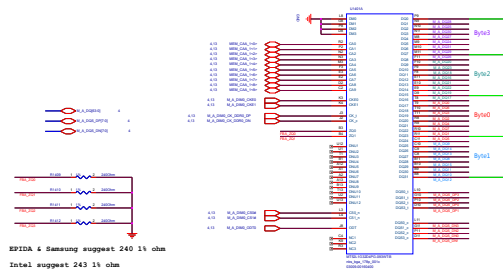
+VCCCORE DeCap
0201 1uF/6.3V X5R h14 *30
0402 10uF/6.3V X5R h13 * 9



Close to LPDDR3 termination resistance (0402 size)



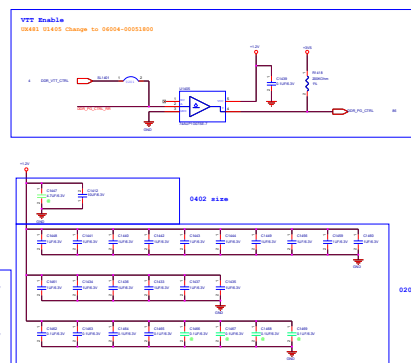
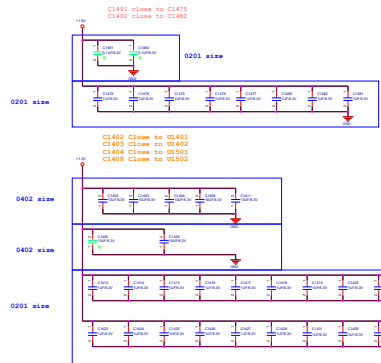
SDP - v00-1305_00_pcap (page141)



LPDDR3 x32 Power Plane Decoupling

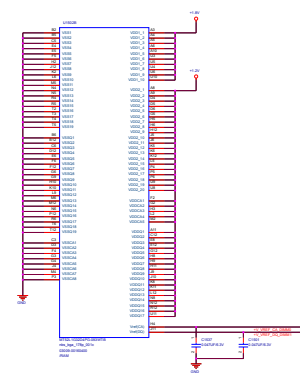
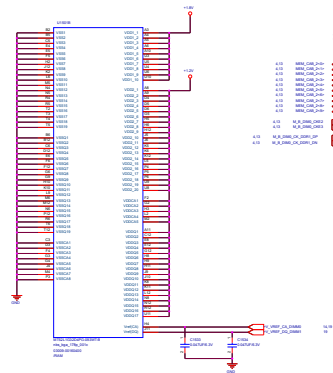
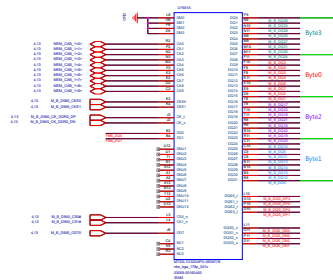
Memory Configuration	Power Domain	Decoupling Location	Qty x pF (size)	Note
LPDDR3 Memory Bank x32 - 2 Devices per Channel	VDDQ	2 near each device, Figure 4-55, VDDQ red circles	8x 0.1µF (0501)	2
		4 near each device, Figure 4-55, VDDQ red circles	18x 1µF (0402)	2
		2 near each device, Figure 4-55, VDDCA yellow circles	8x 1µF (0402)	2
		3 near each device, Figure 4-55, VDD0 blue circles	12x 1µF (0402)	2
		2 near each device, Figure 4-55, VDD0 pink circles	8x 1µF (0402)	2
	VTT	5 Distributed, VDDQ red circles Figure 4-56	5x 10µF (0603)	2
		3 Distributed, VDDCA yellow circles Figure 4-56	3x 10µF (0603)	2
		5 Distributed, VDD0 blue circles Figure 4-56	5x 10µF (0603)	2
		5 Distributed, VDD0 pink circles Figure 4-56	5x 10µF (0603)	2
		Distributed along terminations, Edge or 90° related, Caps shown in green Figure 4-57	8x 1µF (0402)	

Notes:
1. Total quantity is referring to 2 channels.
2. Distributed among the 4 LPDDR3 Devices



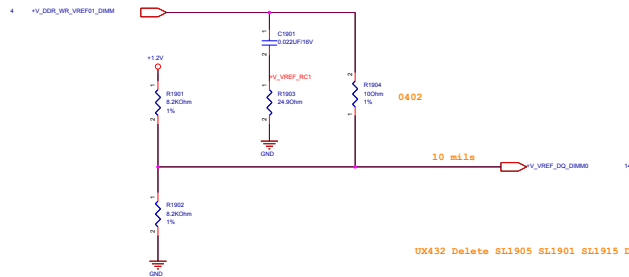


EVITA & Samsung suggest 240 1% ohm
Intel suggest 243 1% ohm



Power plan:1.2V

CHA - VREF_DQ (All close to memory)



CHB - VREF_DQ (All close to memory)

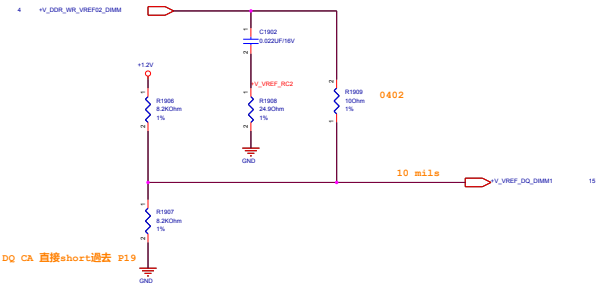
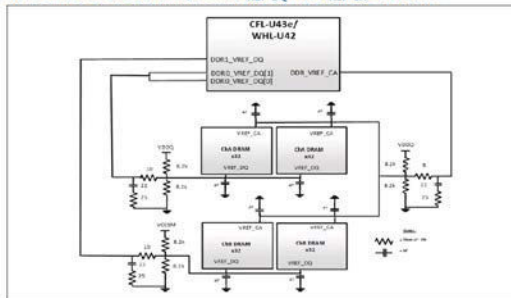
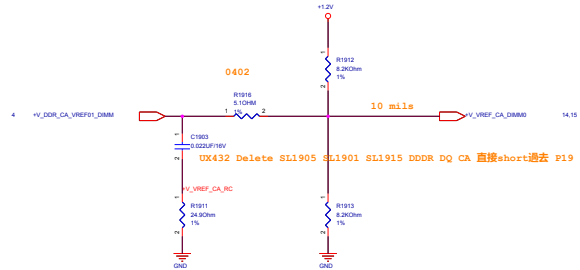
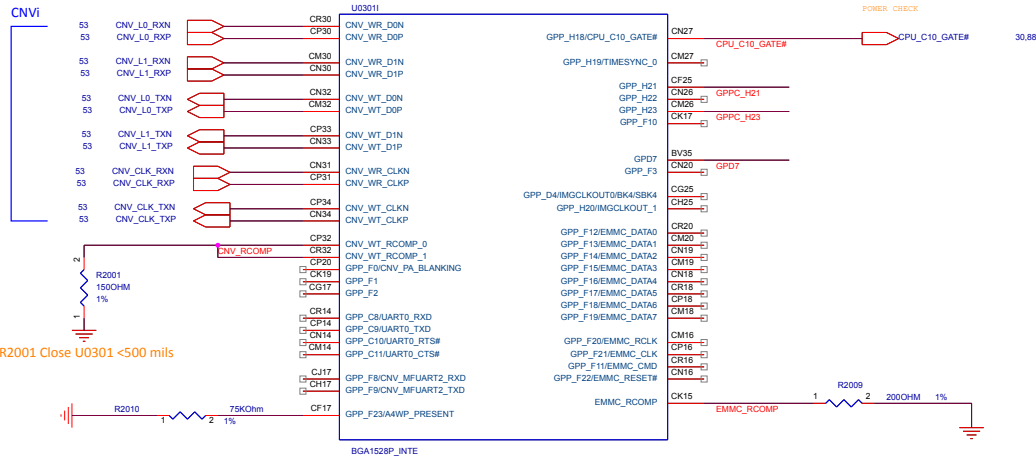


Figure 3-1. WHL U LPDDR3 x32 Memory Down VREF-DQ and VREF-CA Overview

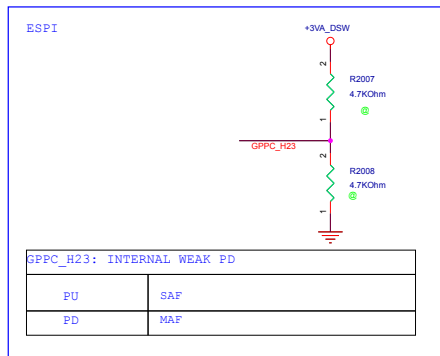


VREF_CA (All close to memory)





R2001 Close U0301 <500 mils



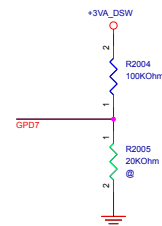
UX432UA Change Follow CRB

CFL CRB v0.8 page#44



GPPC_H21:

PU	24Mhz
PD	38,4/19.2MHZ

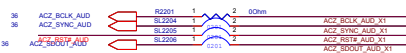


GPD7:

PD	XTAL INPUT IS SINGLE ENDED
PU	XTAL IS ATTACHED

HD Audio

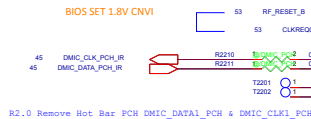
RN2201 near PCH



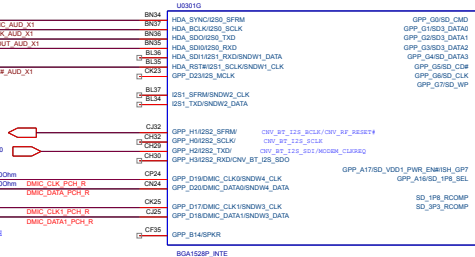
UX432 Mount



BIOS SET 1.8V CNVI



R2.0 Remove Hot Bar PCH DMIC_DATA1_PCH & DMIC_CLK1_PCH



R1.1 add R2209 SD Rcomp PDG285 CRB

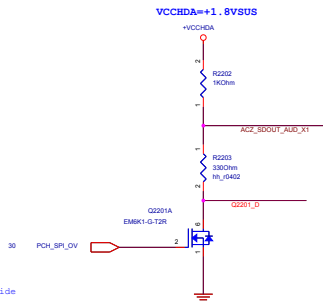
FLASH DESCRIPTOR STRAP

EDS 31.7.1.3

HDA SDO
0=Enable
1=Disable Override

ACZ_SDOUT:(1) PCH: Internal PD 20k
ohm, VIL=0.35V, VIH=0.65*3.3V (2)
ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V

ACZ_SDOUT is a signal used for Flash
Descriptor security Override/MS debug mode
HIGH : get override, LOW : disable override



Intel: To enable Flash Descriptor Security Override, this
signal should be pulled up to VCCCHDA through a 1
kΩ to 2.2 kΩ ±5% resistor.

Top-Block Swap Override

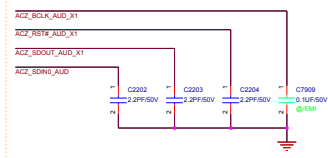
Remove 0429

EDS 4.3.1

PCH_GPPB14: weak internal pull down

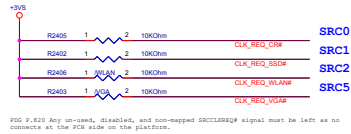
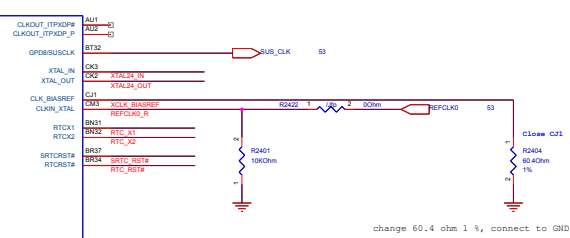
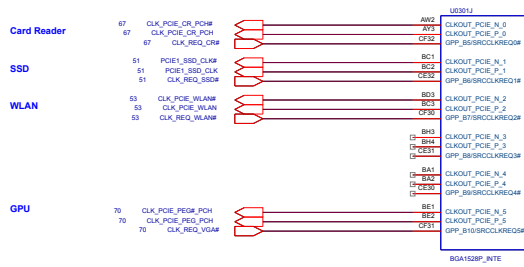
FU	Enable
PD	Disable (default)

C2202,C2203,C2204, WHL PDG: 2.2PF

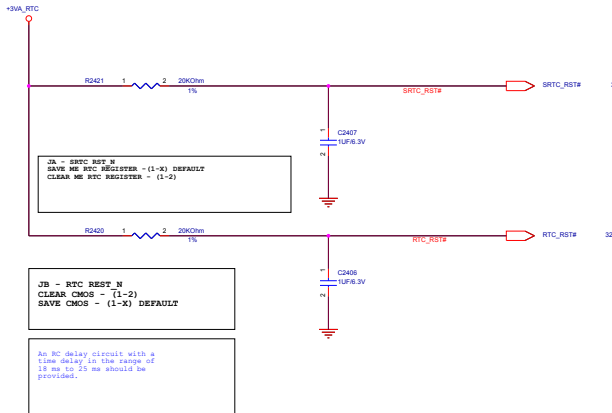


CNVI INTEL Feedback





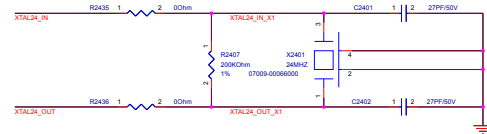
P0D_P0D0 Any un-used, disabled, and non-mapped SRCCLKREQ0W signal must be left as no connects at the PCB side on the platform.



UX333 Reference UX433FDX change to 27PF

XTAL 24MHz

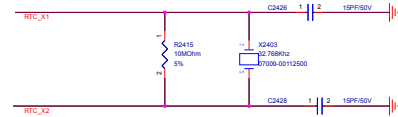
07009-00066000
 07009-00066000



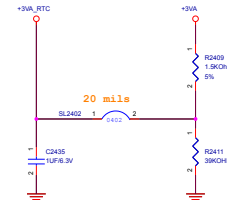
UX333 Reference UX433FDX change to 15PF

RTC XTAL 32.768KHz

07009-00112500
 07009-00113600

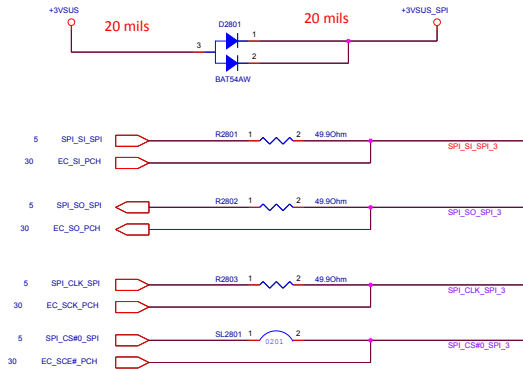


No RTC

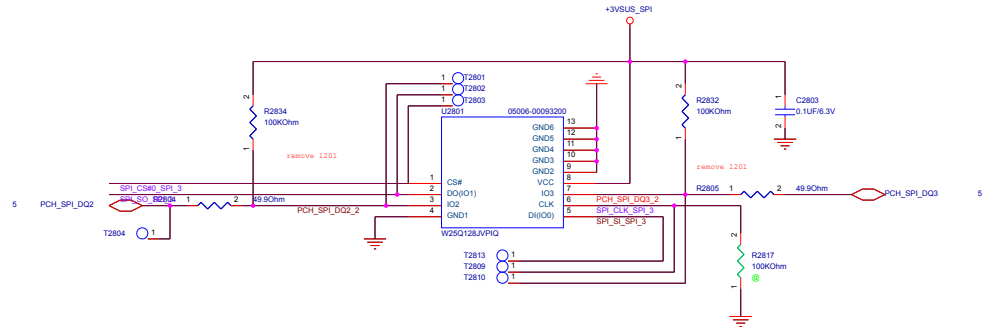


+V3A_RTC GENERATION

SPI PCH Power



PCH SPI 128M (for IT8225)



Main:05006-00093200

2nd:05006-00093700

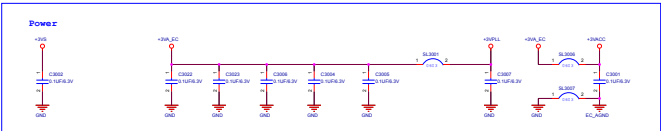
System Management Interface

EC 8995
Only 3V Tolerance
 C9B[0..1,2,3,4,5,6]
 GPC[3,4,5,6,7]
 GPE[4,5,6,7]
 GPF[6,7]
 GPG[7]
 GPH[7]
 GPI[0..7]
 GPO[0..7]

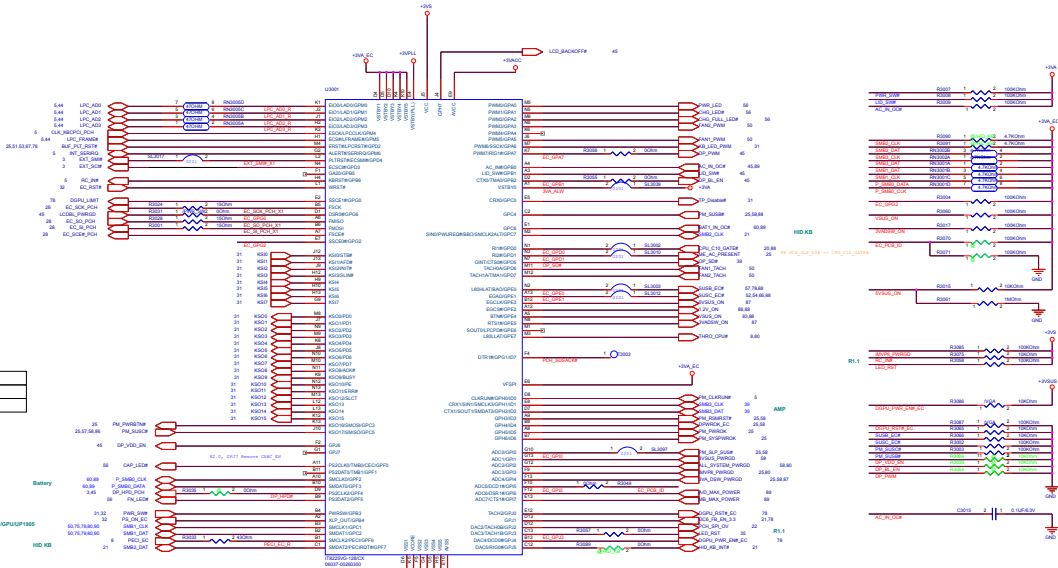
Can be adjusted to
 Open-Drain for ports

GPD0-GPA3
 GPD0-GPD7
 GPD0-GPD7
 GPD0-GPD7
 GPD0-GPD7
 GPD0-GPD6
 GPD0-GPD5

EC Require



DS4310 Initiate +3Vn_EC C9B02 100P C9C03 100P

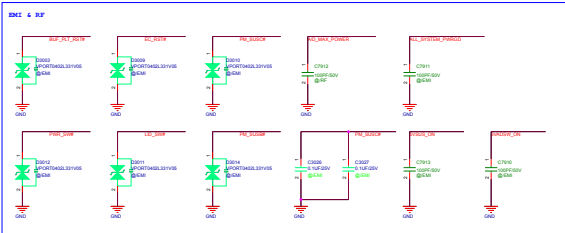


ITE Version	AS08 P/N
179225V0-128/CX	06037-00260300

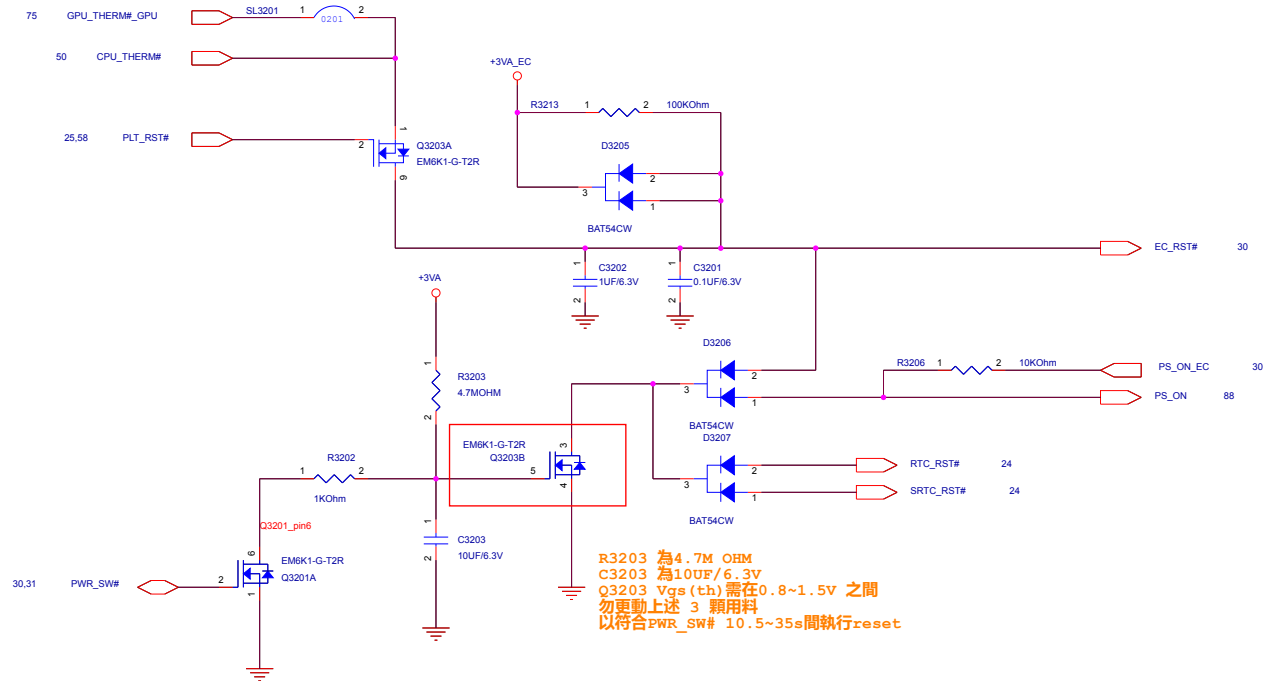
Battery

Thermal sensor GPDS0055

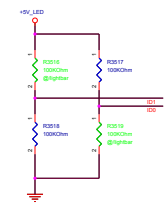
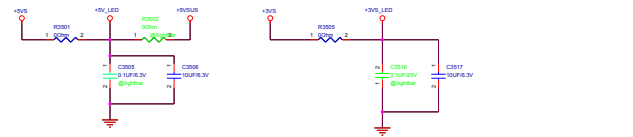
HD XB



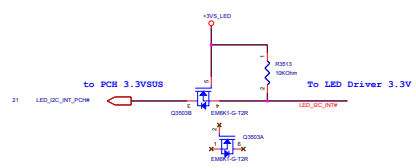
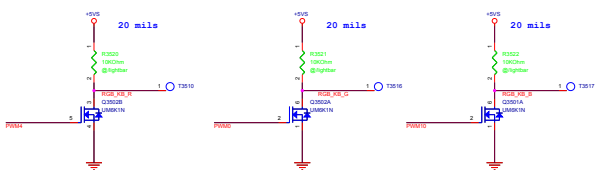
Thermal Policy



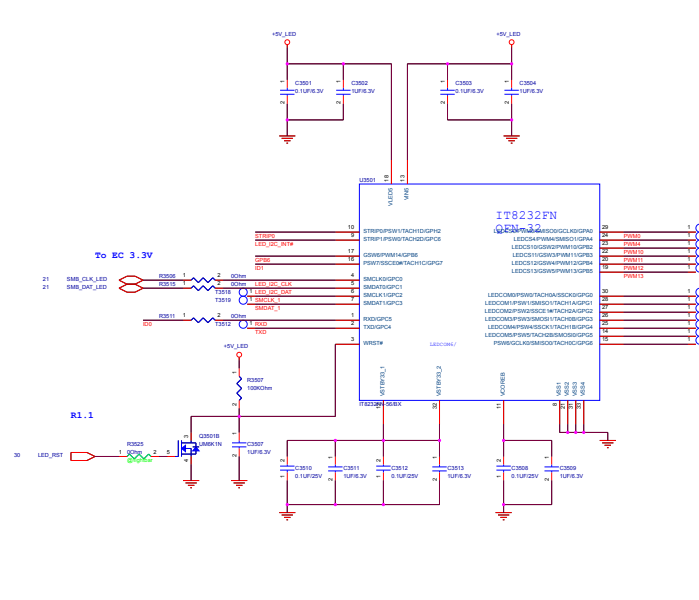
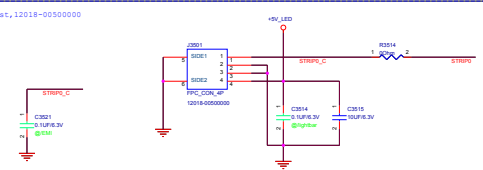
battery embedded (press pwr_sw 40sec, then reset ec & RTC)



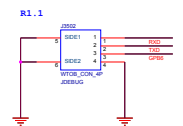
ID0	ID1	Feature
L	L	5 LEDs
L	H	1 LEDs
H	L	STRIP
H	H	



1st, 12018-00500000



For Debug Used 1220
1st, 12017-00380100



STRIP

The image contains three circuit diagrams illustrating different MOAT connection methods:

- Diagram 1:** A single MOAT component. The Digital input (pin 1) is connected to a 5V supply. The Analog input (pin 2) is connected to a 5V supply. The output (pin 3) is connected to a 5V supply. The ground (pin 4) is connected to ground.
- Diagram 2:** Two MOAT components, labeled AVDD1 and AVDD2+CPVDD. The Digital input (pin 1) of AVDD1 is connected to a 5V supply. The Analog input (pin 2) of AVDD1 is connected to a 5V supply. The output (pin 3) of AVDD1 is connected to a 5V supply. The ground (pin 4) of AVDD1 is connected to ground. The Digital input (pin 1) of AVDD2+CPVDD is connected to a 5V supply. The Analog input (pin 2) of AVDD2+CPVDD is connected to a 5V supply. The output (pin 3) of AVDD2+CPVDD is connected to a 5V supply. The ground (pin 4) of AVDD2+CPVDD is connected to ground.
- Diagram 3:** A single MOAT component. The Digital input (pin 1) is connected to a 5V supply. The Analog input (pin 2) is connected to a 5V supply. The output (pin 3) is connected to a 5V supply. The ground (pin 4) is connected to ground.

The top diagram shows the connection for the +1.8V_AVS_2VDD_I/O pin. It is connected to a 1.8V source through a 3k3 resistor. The pin is labeled "Place next to PIN19". The internal circuitry shows a capacitor C3629 (100nF) connected to the pin and a 1uF capacitor connected to the 1.8V source.

The bottom diagram shows the connection for the +0.9V_AVS_2VDD pin. It is connected to a 0.9V source through a 3k3 resistor. The pin is labeled "Place next to PIN3". The internal circuitry shows a capacitor C3631 (100nF) connected to the pin and a 1uF capacitor connected to the 0.9V source.

		DYD0 (1.8V/3.3V)	DYD0-IO (0.5V/3.3V)	AYD00 (0V)	AYD00+PTD0 (0.5V)	PTD00/2 (0V)	Total Power
		(mW)	(mW)	(mW)	(mW)	(mW)	(mW)
1	DYD0-1.8V, DYD0-IO-1.5V	3.399	0.0897	14.45	70.4	100	5505.14775
2	DYD0-3.3V, DYD0-IO-3.3V	5.905	0.172	14.46	70.66	100	5610.375

Headphone

PCB trace width of Ring2 & SLEEVE at least 40 mil

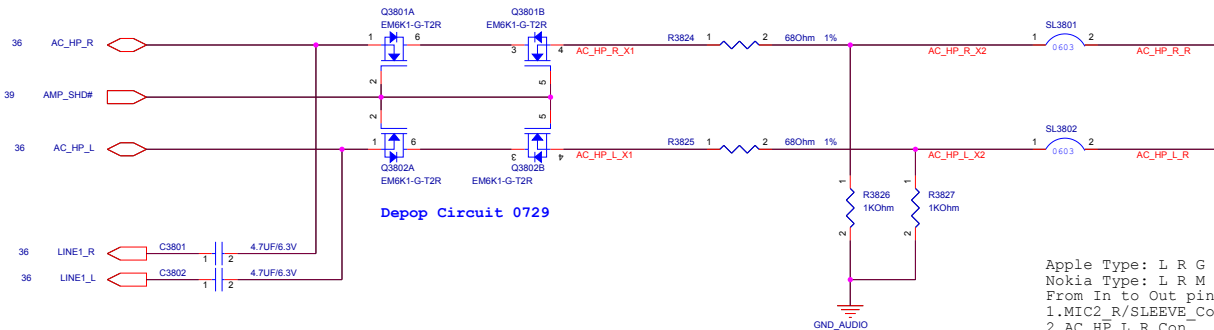
DMIC

R646 1 0 R647 DMIC_CLK DMIC_CLK_R 45
C647 C648 DMIC_DATA DMIC_DATA_R 45

R2.C Remove Rot Bar DMIC_DATA & DMIC_DATA34

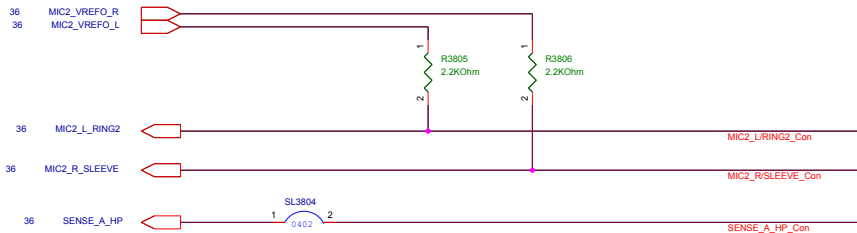
[illegible]

20 mils

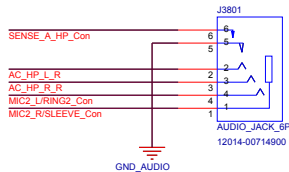


Apple Type: L R G M
 Nokia Type: L R M G
 From In to Out pin define:
 1.MIC2_R/SLEEVE_Con
 2.AC_HP_L_R_Con
 3.AC_HP_R_R_Con
 4.MIC2_L/RING2_Con

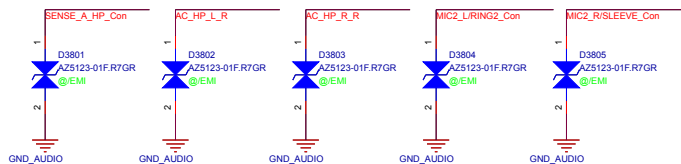
10 mils



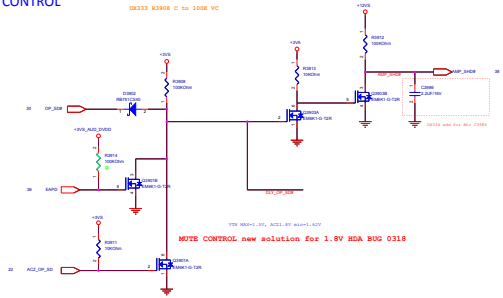
40 mils



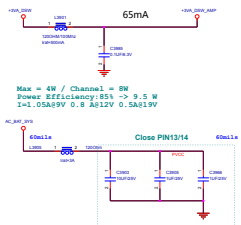
Phone Jack ESD



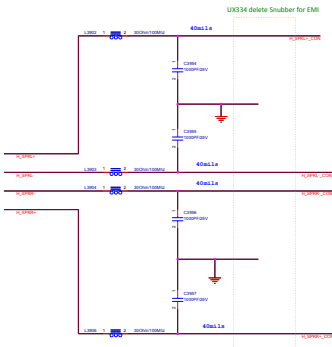
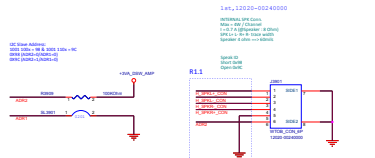
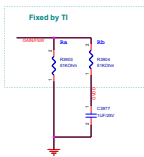
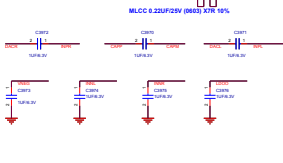
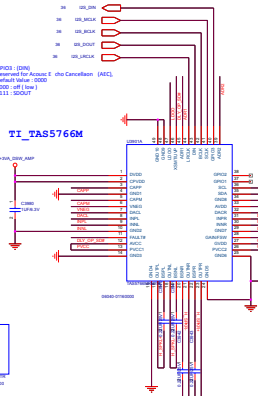
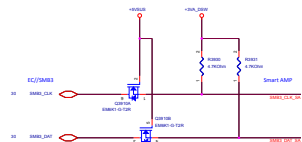
MUTE CONTROL



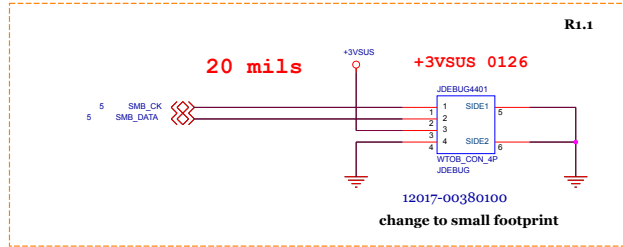
Smart AMP Power



System Management Interface



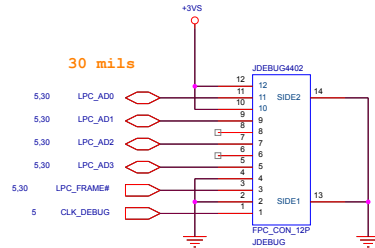
New Design Debug Port

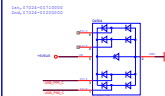
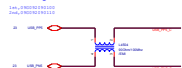
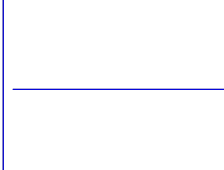
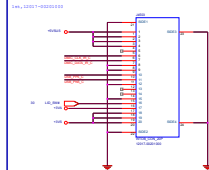
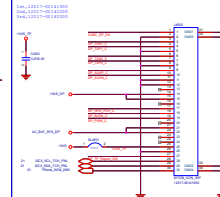
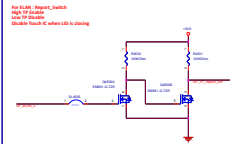
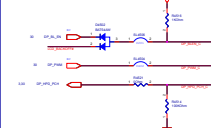
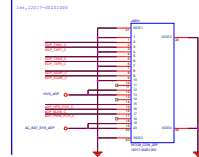
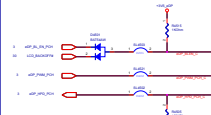
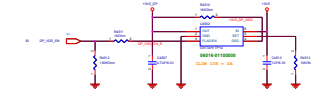
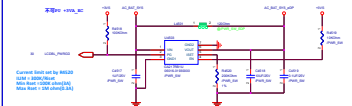
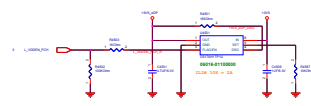


LPC Debug Port

Follow UX370UAR

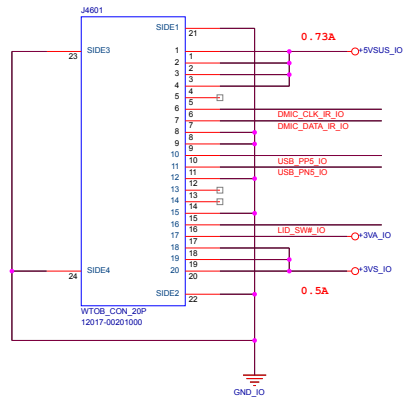
12018-00102300





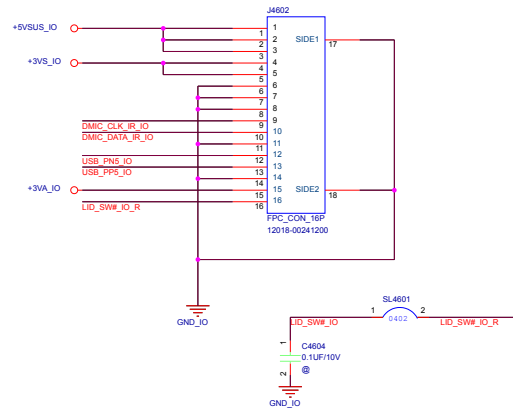
DMIC//IR//HALL Connector

1st,12017-00201000



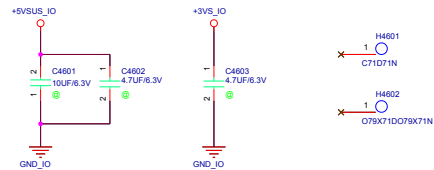
IR Connector

1st,12018-00241200



DMIC CLK Signal

R2.0 Remove Hot Bar DMIC_CLK



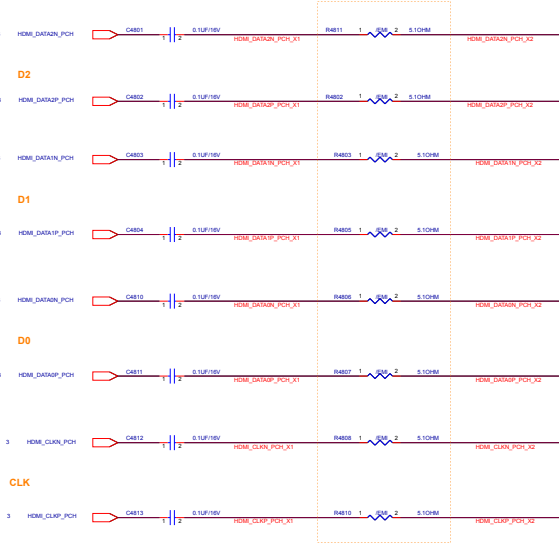
DMIC Connector

1st,12018-00082900

R2.0 Remove Hot Bar DMIC Connector & DMIC_DATA_IO

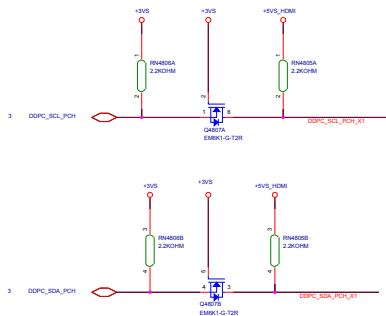


HDMI Signals

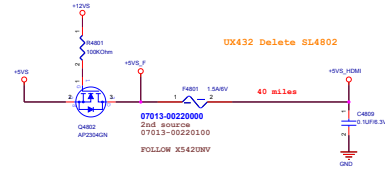


HDMI DDC Level-shifter

UX432 Delete D4801 D4802

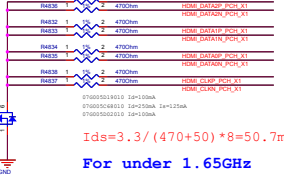
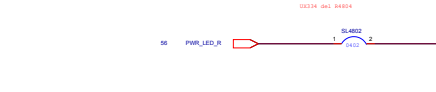


HDMI Power



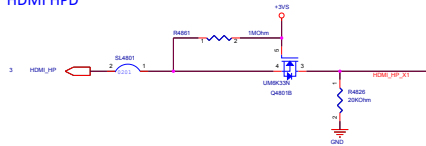
HDMI Cost-reduced Level shifter

UX432 Delete KB_PWR_LED_EM_GPIO_P15 D4801 D4802 D4803 D4804 D4805 D4806 D4807 D4808 D4809 D4810 D4811 D4812 D4813 D4814 D4815 D4816 D4817 D4818 D4819 D4820 D4821 D4822 D4823 D4824 D4825 D4826 D4827 D4828 D4829 D4830 D4831 D4832 D4833 D4834 D4835 D4836 D4837 D4838 D4839 D4840 D4841 D4842 D4843 D4844 D4845 D4846 D4847 D4848 D4849 D4850 D4851 D4852 D4853 D4854 D4855 D4856 D4857 D4858 D4859 D4860 D4861 D4862 D4863 D4864 D4865 D4866 D4867 D4868 D4869 D4870 D4871 D4872 D4873 D4874 D4875 D4876 D4877 D4878 D4879 D4880 D4881 D4882 D4883 D4884 D4885 D4886 D4887 D4888 D4889 D4890 D4891 D4892 D4893 D4894 D4895 D4896 D4897 D4898 D4899 D4900 D4901 D4902 D4903 D4904 D4905 D4906 D4907 D4908 D4909 D4910 D4911 D4912 D4913 D4914 D4915 D4916 D4917 D4918 D4919 D4920 D4921 D4922 D4923 D4924 D4925 D4926 D4927 D4928 D4929 D4930 D4931 D4932 D4933 D4934 D4935 D4936 D4937 D4938 D4939 D4940 D4941 D4942 D4943 D4944 D4945 D4946 D4947 D4948 D4949 D4950 D4951 D4952 D4953 D4954 D4955 D4956 D4957 D4958 D4959 D4960 D4961 D4962 D4963 D4964 D4965 D4966 D4967 D4968 D4969 D4970 D4971 D4972 D4973 D4974 D4975 D4976 D4977 D4978 D4979 D4980 D4981 D4982 D4983 D4984 D4985 D4986 D4987 D4988 D4989 D4990 D4991 D4992 D4993 D4994 D4995 D4996 D4997 D4998 D4999 D5000



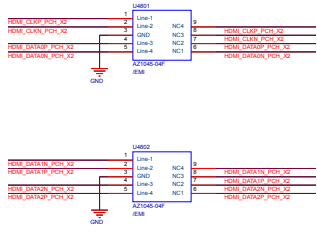
$I_{ds} = 3.3 / (470 + 50) * 8 = 50.7mA$
For under 1.65GHz

HDMI HPD



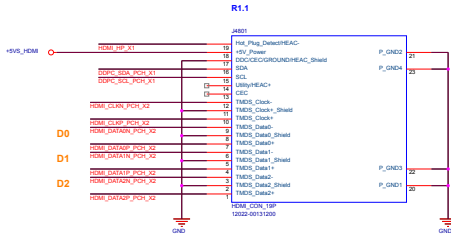
HDMI ESD

0701000100100

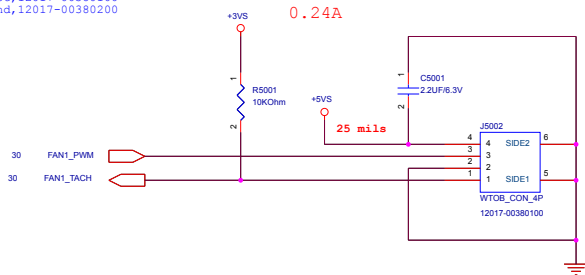


HDMI CON.

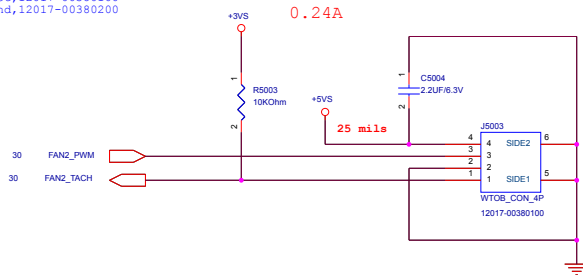
141-12022-00131200
2nd, 12022-00131300



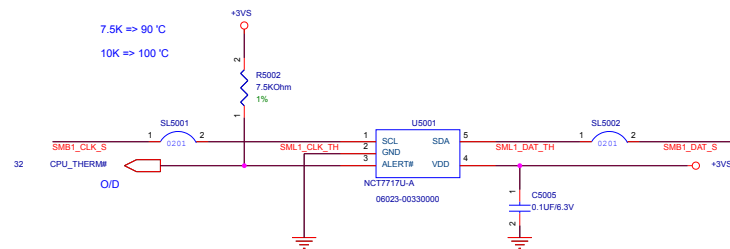
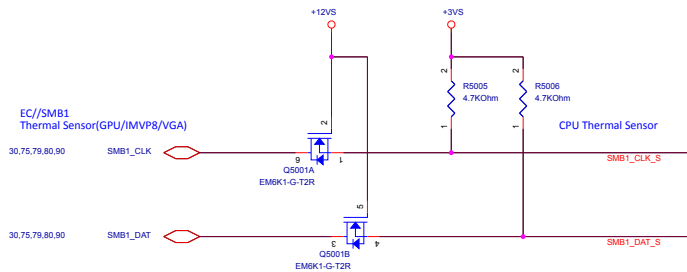
1st, 12017-00380100
2nd, 12017-00380200



1st,12017-00380100
2nd,12017-00380200



CPU Thermal Sensor



NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

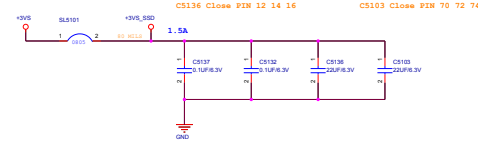


Table 36-7. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

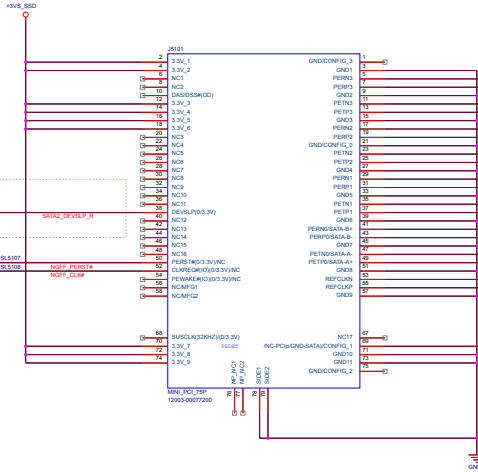
Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA only	PCI Express® Gen 2 / SATA	PCI Express® Gen 3 / SATA
Processor Ta	180 nF	220 nF	50 nF	180 nF	220 nF
Processor Pa	None	None	10 nF ¹	None	None ¹

SATA DEVSLP.

Delete SATA2_DEVSLP_R R5317 0 ohm ADD SL5102 short x5101 0ohm nonDEVSLP P51

25.30.53.67.78
24

SLF_P1T_RST#
CIA_REQ_SIG#



UX432 Delete R55103 (CS199 R5105 MSATA_MPCIE_DET# (UX370)
PULL HIGH PCH Side R2302
PCIE : N.C
SATA : GND

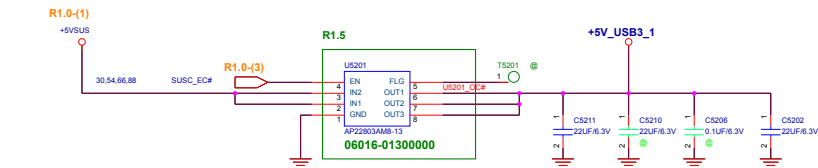
L3

L2

L1

L0

USB3.0 Power Switch

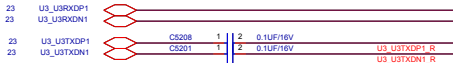


MSOP-8 PWR Switch of New Pool List :
1st : P/N: 06016-01300000 POWER SW. AP22803AM8-13/DIODES MSOP-8.
2nd : P/N: 06G030046024 POWER SW. G547E1P81U/GMT MSOP8.

USB3.0 Signal

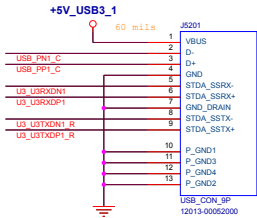
BCM 109022~00110000

R1.1, Remove EMPASS
R2.0, Remove RN5204 & RN5205 (10G302000004030)



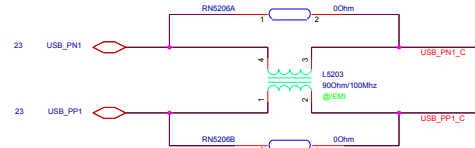
USB3.0 Type A Connector (GEN2_10G)

1st,12013~00052000



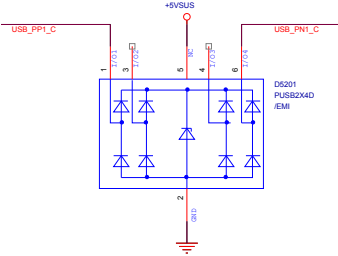
USB 2.0 Signal & Common choke Protection

1st,09G092090100
2nd,09G092090110



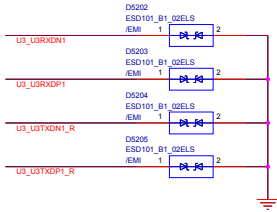
USB2.0 ESD-Protection

1st,07024~00710000
2nd,07024~00200200

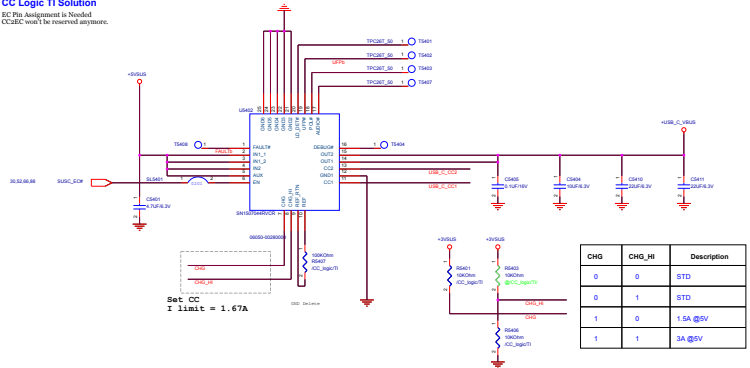


USB3.0 ESD-Protection

07024~01050000



CC Logic TI Solution EC Pin Assignment is Needed CCMC won't be reserved anymore.



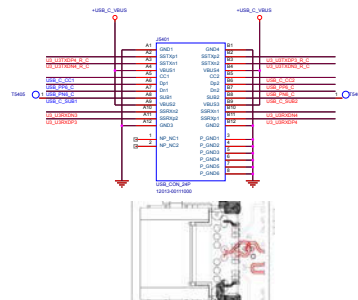
USB3.0 Common choke RF

R1..1, Resistor R05022
R2..1, Resistor R05401, R05402, R05403 & R05404 (10030200004030)



Type-C Connector

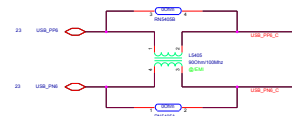
147p, 12011-001110002
27nF, 12013-00116300
27nF, 12013-00113500



the stub of USB2.0 needs to be as short as possible which is shown as below

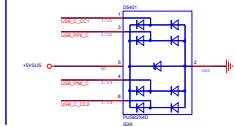
USB 2.0 Common choke EMI-Protection

1nF, 090502000105
2nF, 090502000110



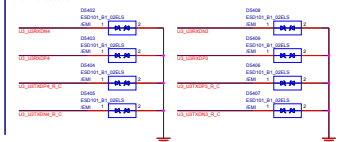
USB 2.0 ESD-Protection

1nF, 07024-00710005
2nF, 07024-00200200



USB3.0 ESD-Protection

07024-00200005



[illegible]

31

PR KB PWRLED Connect

PWR_LED

RS640

EM80K1-G-T2R
G90Y1B

POWER_LED_R

PR DEL @RS640 Change to 330 ohm

31

PWR_LED

RS604

ISHOMK

PWR_LED_R

C560
10Vf IRV

Mn_020V_014

PR DEL @RS601

48

1st.07014-00114200

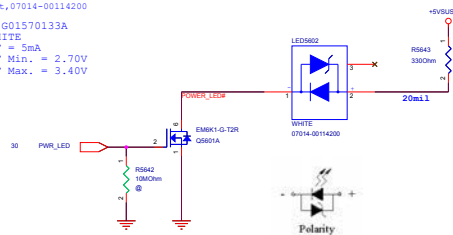
07G01570133A

WHITE

 $I_F = 5\text{mA}$

VF Min. = 2.70V

VF Max. = 3.40V



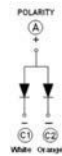
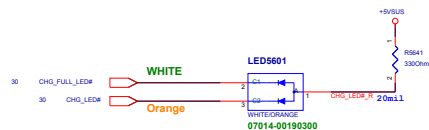
1st, 07014-00190300

1st, 07014-00190300

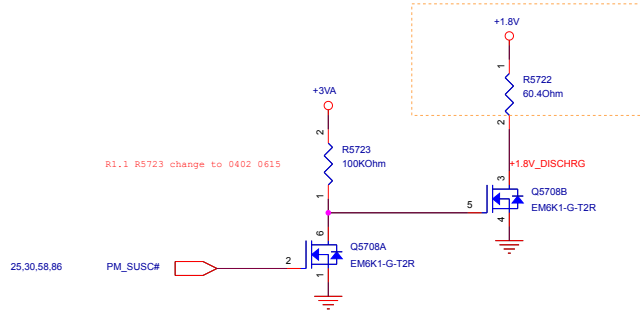
WHITE (FULL)

IF (max) = 20mA

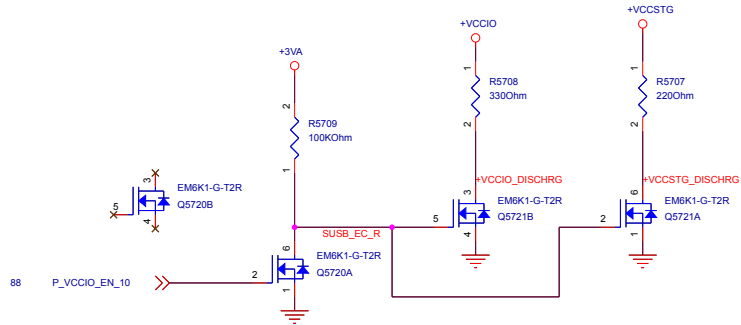
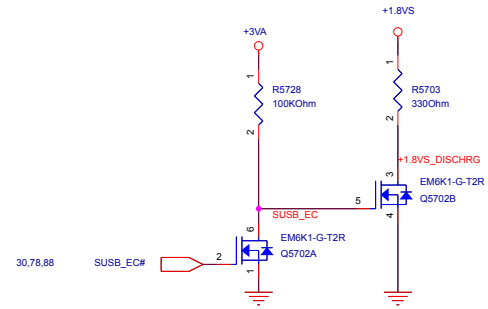
VF Max. = 3.15V (@IF=5mA)



+1.2V Change to +1.8V



VS discharge



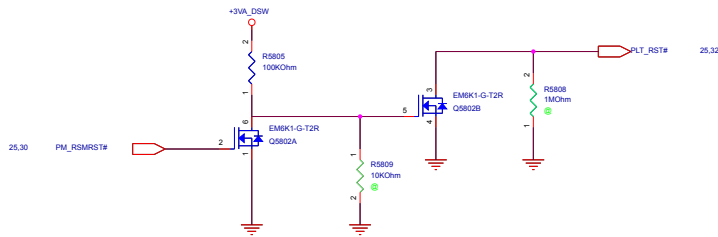
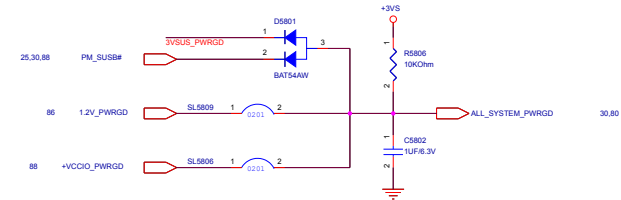
DEL +1.05VSUS Discharge

3VSUS_PWRGD

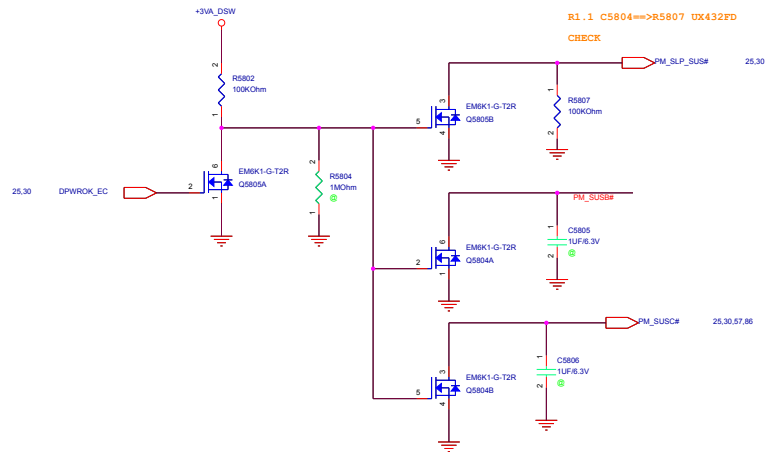
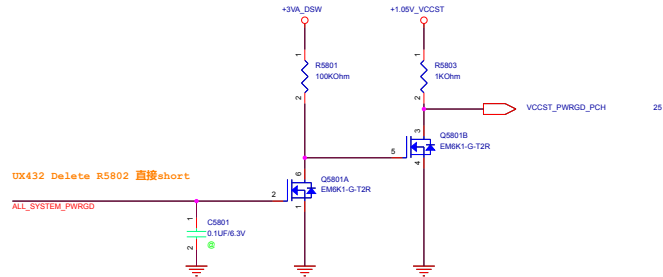
UX432 R1.1 Delete @D5804

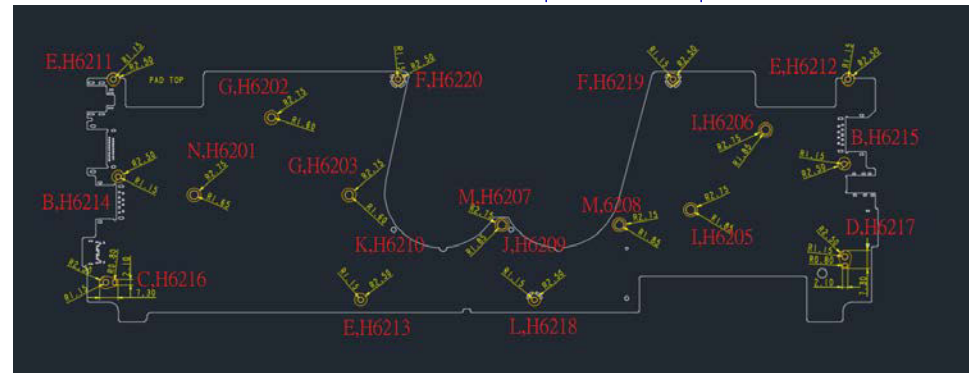
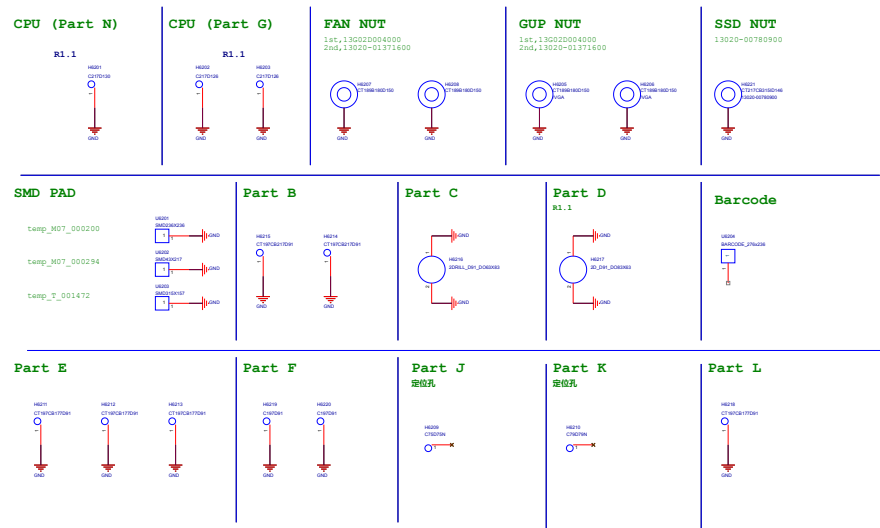


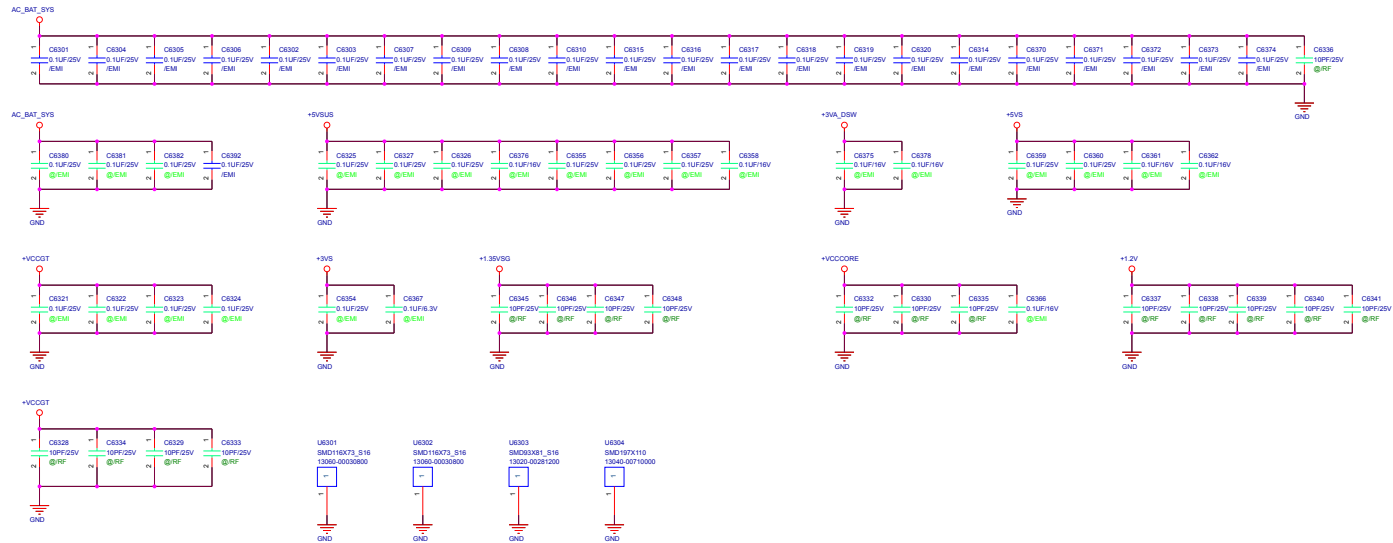
ALL_SYS_PWRGD



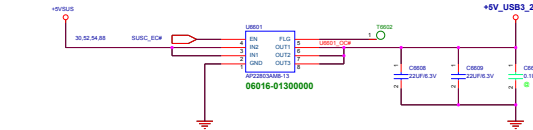
VCCST_PWRGD for PCH





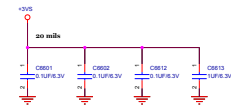


USB3.0 Power Switch



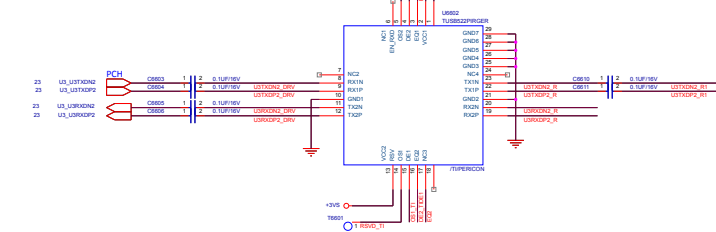
USB3.0 Power Re-Driver

Power Normal
327 mW → 99 mA



USB3.0 Signal Re-Driver

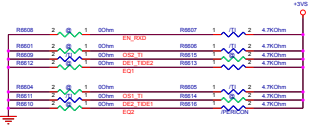
PERCON : 0613-00180100 (P0607500M)
TI : 06113-00240000 (TUS8522P0RGER)



USB3.0 Signal

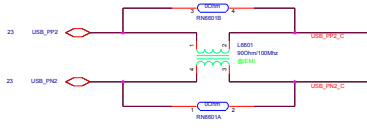
ROM : 09022-00110000
S2: 0, Remove EMPASS 16602 & 16603
R2: 0, Remove R80401, R80402, R80403 & R80404 (106302000004030)

< EQ / DE > and < Other Pin Funcon >



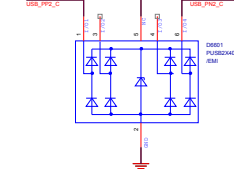
USB 2.0 Signal & Common choke Protection

1st, 0902020010000
2nd, 09020200100



USB2.0 ESD-Protection

1st, 07024-001000000
2nd, 07024-00200000



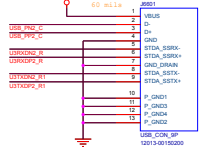
USB3.0 ESD-Protection

07024-01000000

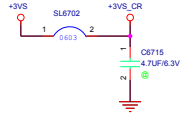


USB3.0 Type A Connector (GEN1_5G)

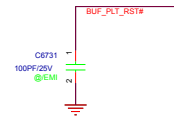
1st, 12013-001000000



Power Trace:
+3VS_40 mils source
+3VS_CR 40 mils
+3VS_CARD_F 30 mils
+3VS_CARD 30 mils



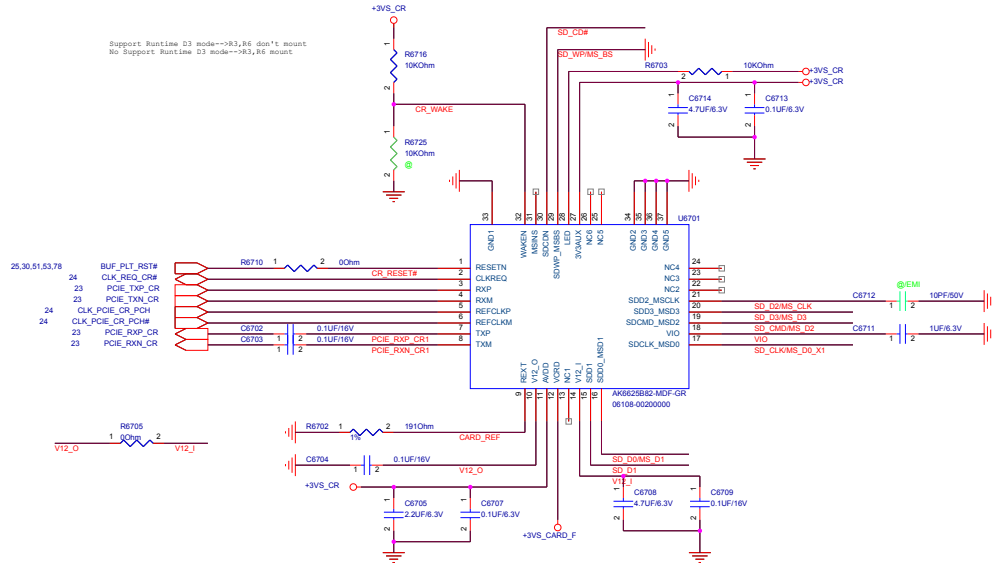
EMI



Card Reader IC_AK6625

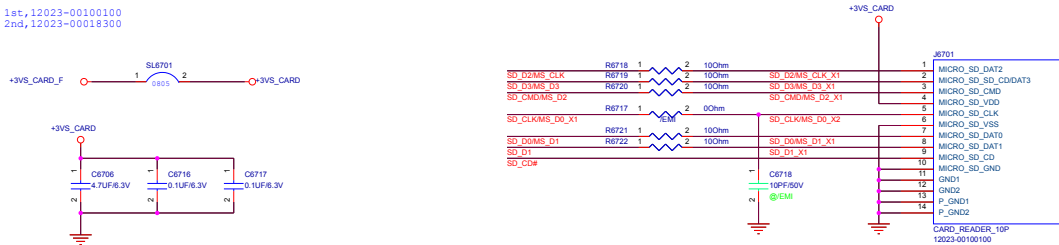
1st,06108-00200000

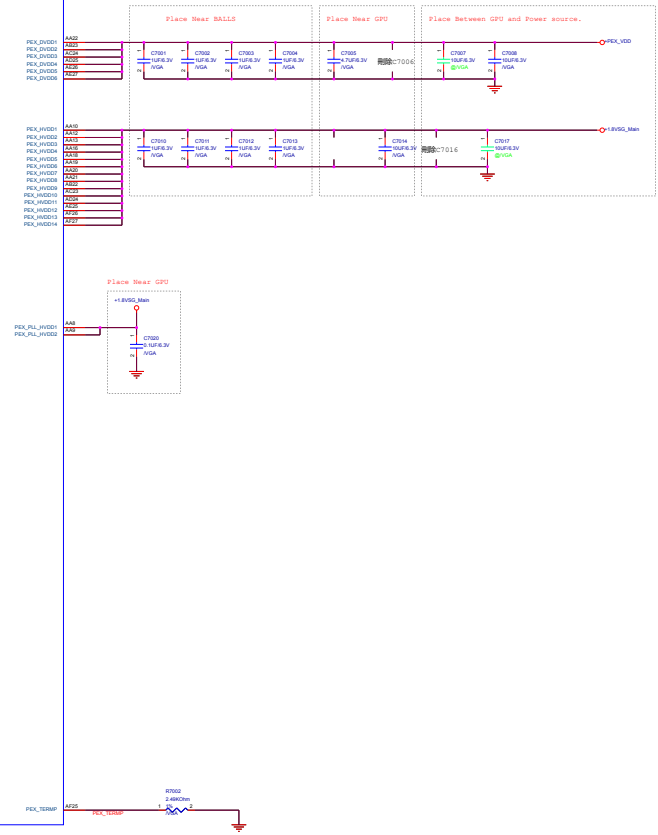
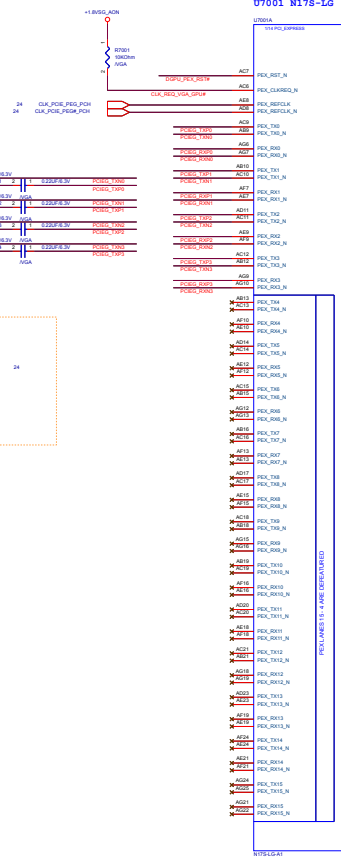
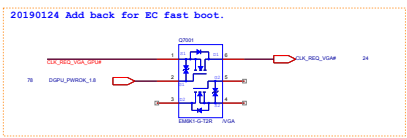
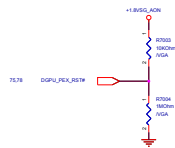
```
Support Runtime D3 mode-->R3,R6 don't mount
No Support Runtime D3 mode-->R3,R6 mount
```



Micro SD Connector

1st, 12023-00100100
2nd, 12023-00018300





GPU MEMORY INTERFACE

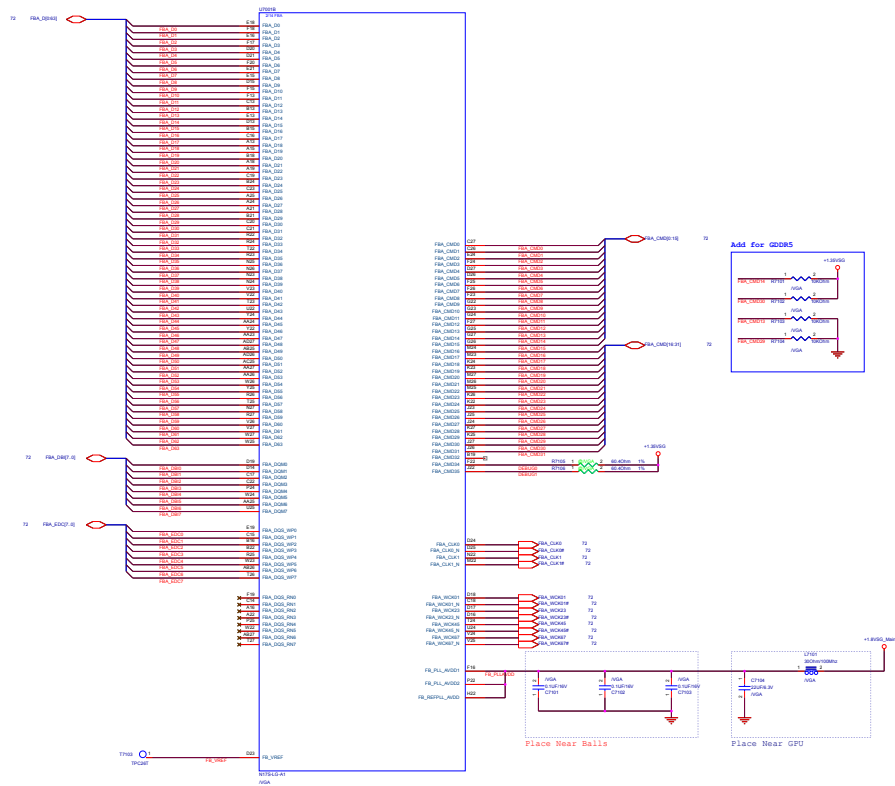
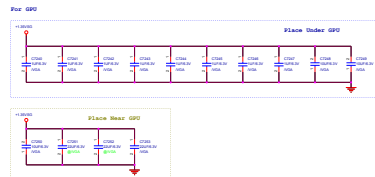
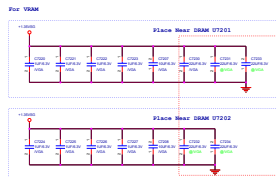
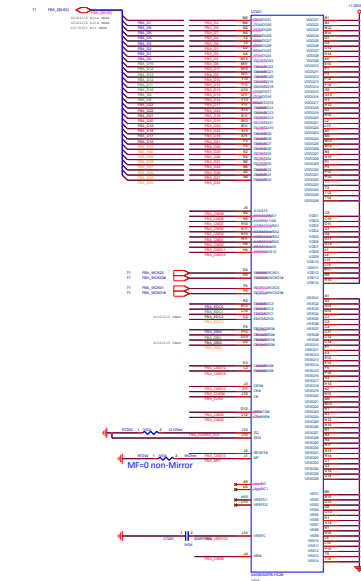
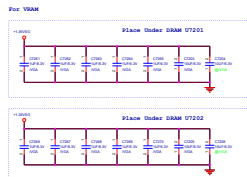
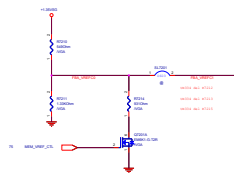
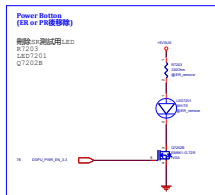
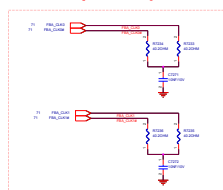


Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	HST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

UX334 GPU memory clock change to 3GHz



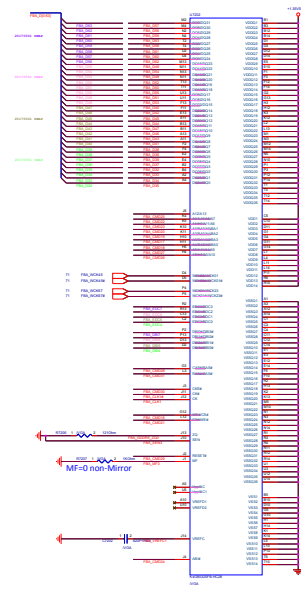
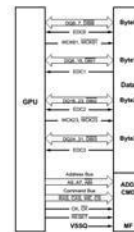
Route at least 2 GND vias
and 2 ground test
for each inductor

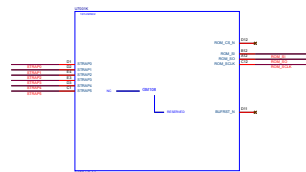
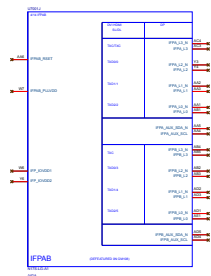
Samsung, GDDR5, 03008-00050000
Micron, GDDR5, 03008-00050000

Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAH Signal Definition
For DRAH(s) tied to DQ(31:0)	For DRAH(s) tied to DQ(43:32)	
FB_A_CMD0	FB_A_CMD16	CS*
FB_A_CMD1	FB_A_CMD17	A3_BA3
FB_A_CMD2	FB_A_CMD18	A2_BA0
FB_A_CMD3	FB_A_CMD19	A1_BA2
FB_A_CMD4	FB_A_CMD20	A5_BA1
FB_A_CMD5	FB_A_CMD21	WE*
FB_A_CMD6	FB_A_CMD22	A7_A8
FB_A_CMD7	FB_A_CMD23	A6_A9
FB_A_CMD8	FB_A_CMD24	A0*
FB_A_CMD9	FB_A_CMD25	A12_SF0
FB_A_CMD10	FB_A_CMD26	A0_A10
FB_A_CMD11	FB_A_CMD27	A1_A9
FB_A_CMD12	FB_A_CMD28	RAS*
FB_A_CMD13	FB_A_CMD29	RS1*
FB_A_CMD14	FB_A_CMD30	CK*
FB_A_CMD15	FB_A_CMD31	CAS*

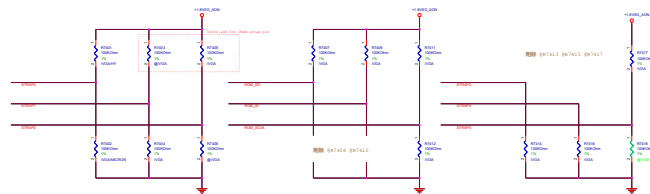
~100m



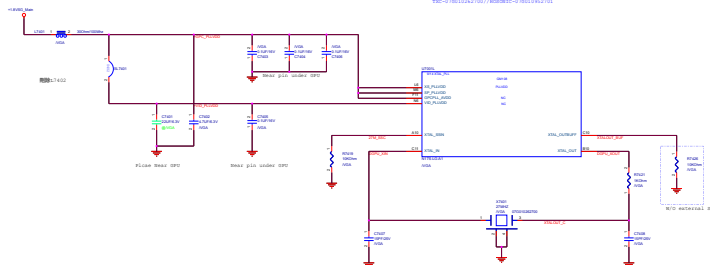


Row Index	Strap Pins see Note			Resulting SOR _X EXPOSED Enablings			
	ROM_S0	ROM_S1	ROM_SCLX	SOR ₃ EXPOSED	SOR ₂ EXPOSED	SOR ₁ EXPOSED	SOR ₀ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
0	H	M	M	disabled	disabled	disabled	disabled

Strap Pins, Note 1			Functions Selected by This Strapping			
STRAP2	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
H	M	M	1	1	1	1



XTAL 27MHz



Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	

Memory Density	Memory Configuration	Frequency	Manufacturer	Die Revision	Strap #	Memory Speed Grade	Data Code Alert	Qual Pin	Status
8 Gb	256Mx32	1.35V	MTD	MTD12500-00-0	0-0	8 Gbps	N/A	N/A	Substitution allowed with warning

- **SMB_ALT_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits (see Section 2.2.1 for the SMBus address).
- **DEVID_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. NVIDIA graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE:** This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

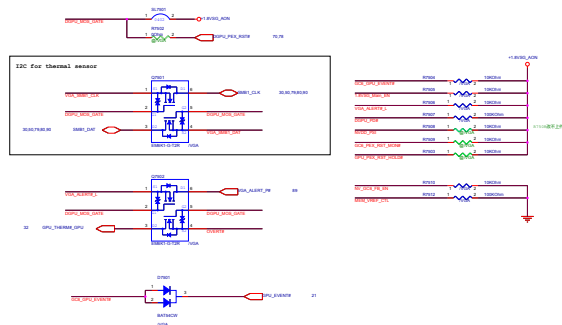
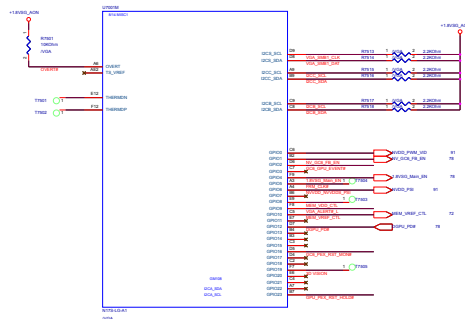


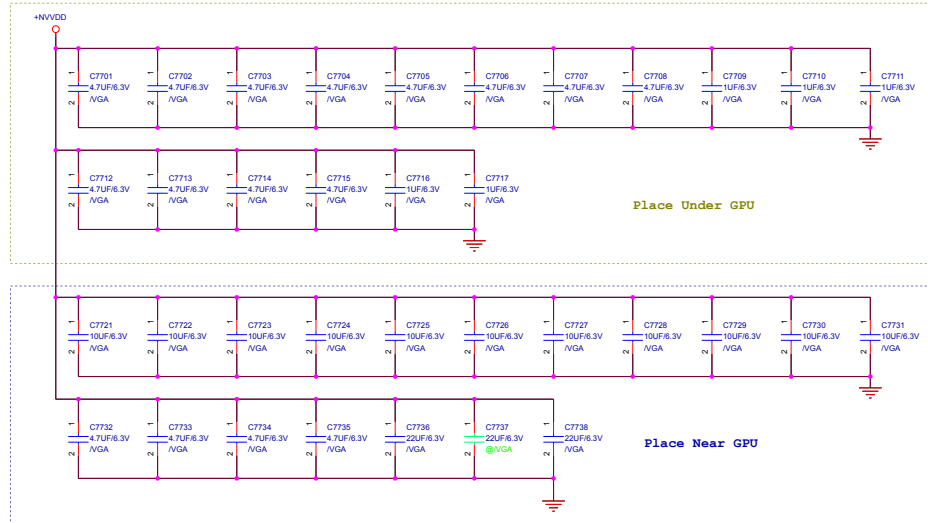
Table 14.1 GPIO Descriptions for GB2C-64 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	LVDD0_PWM	O	PWM Output to control HVDD0	0 to 1V8 PWM output
GPIO1	GCAM: GC6_FB_EH	O	FB Enable for GC6 2.1	Open Source-10 kΩ pull-up to 1V8_AOH unless driven actively.
GPIO2	GCAM: GPU_EVENT*/WAKE*	I	GPU wake signal for GC6 2.1	0 to 1V8 output
GPIO3	HVDD05_PWM	I/O	PWM output to control the HVDD05 power supply	0 to 1V8 output
GPIO4	GCAM: TV8_MAB1_EH	O	GPU power sequencing for GC6 2.1	Open Drain, 10 kΩ pull-up to 1V8_AOH
GPIO5	FRIL_LCK*	I	Active low Frame Lock	Open Drain, 10 kΩ pull-up to 1V8_AOH
GPIO6	HVDD0_PSM*/HVDD05_PSM*	O	Phase Shifting (see Section 14.3.3)	10 kΩ pull-up to 1V8_AOH to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain, 10 kΩ pull-up to 1V8_AOH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down

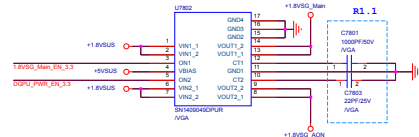
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO11	LCD_VDD Quad*Pwrtr_Brkr*	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AOH
GPIO13	LCD_BLEH	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB*	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GCAM: SYS_PEX_RST_MON*	I	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AOH unless actively driven
GPIO17	UNUSED	I/O		
GPIO18	UNUSED	I/O		
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO21	MEM_VDD_CTL	O	Frame Buffer VDD select	Open Drain; Pull-up/pull-down to set the FBVDD/Q power-on voltage at boot up
GPIO22	UNUSED	I/O		
GPIO23	GCAM: GPU_PEX_RST_HOLD*	O	GPU PCIe self-reset control	Open Drain, 10 kΩ pull-up to gated V13



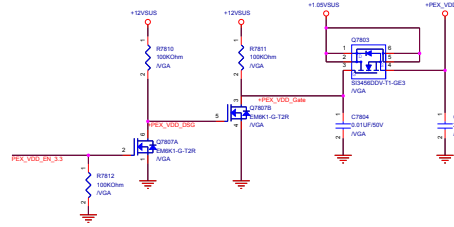
NVDD POWER AND DECOUPLING



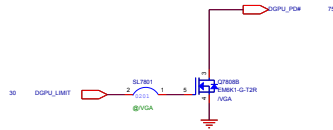
+1.8VSG_AON
+1.8VSG_Main



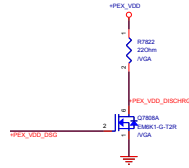
+PEX_VDD



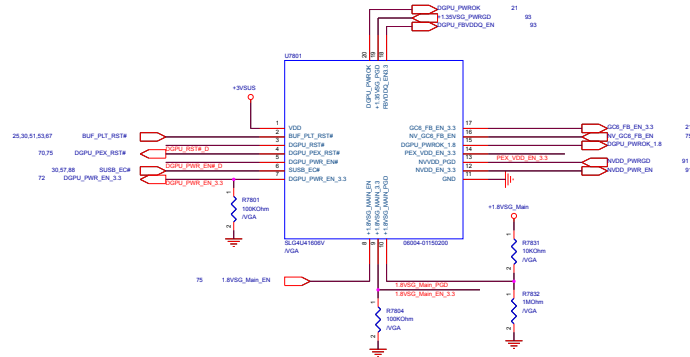
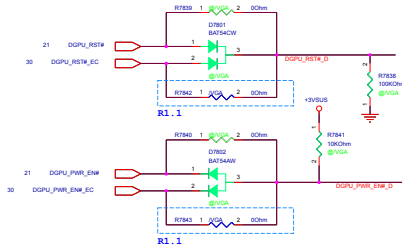
DGPU_PD#



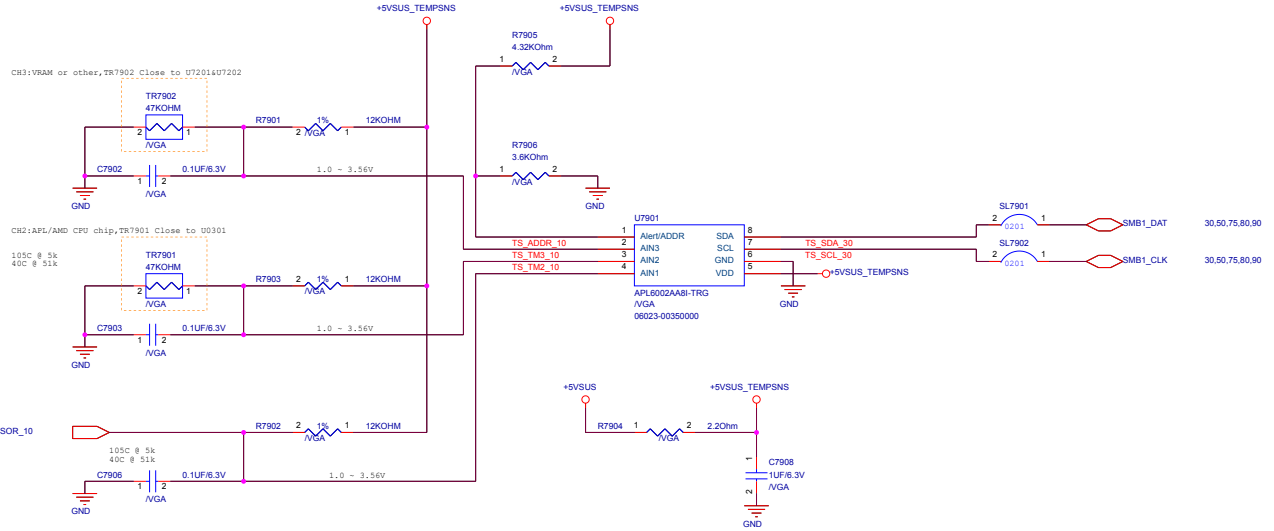
Discharge

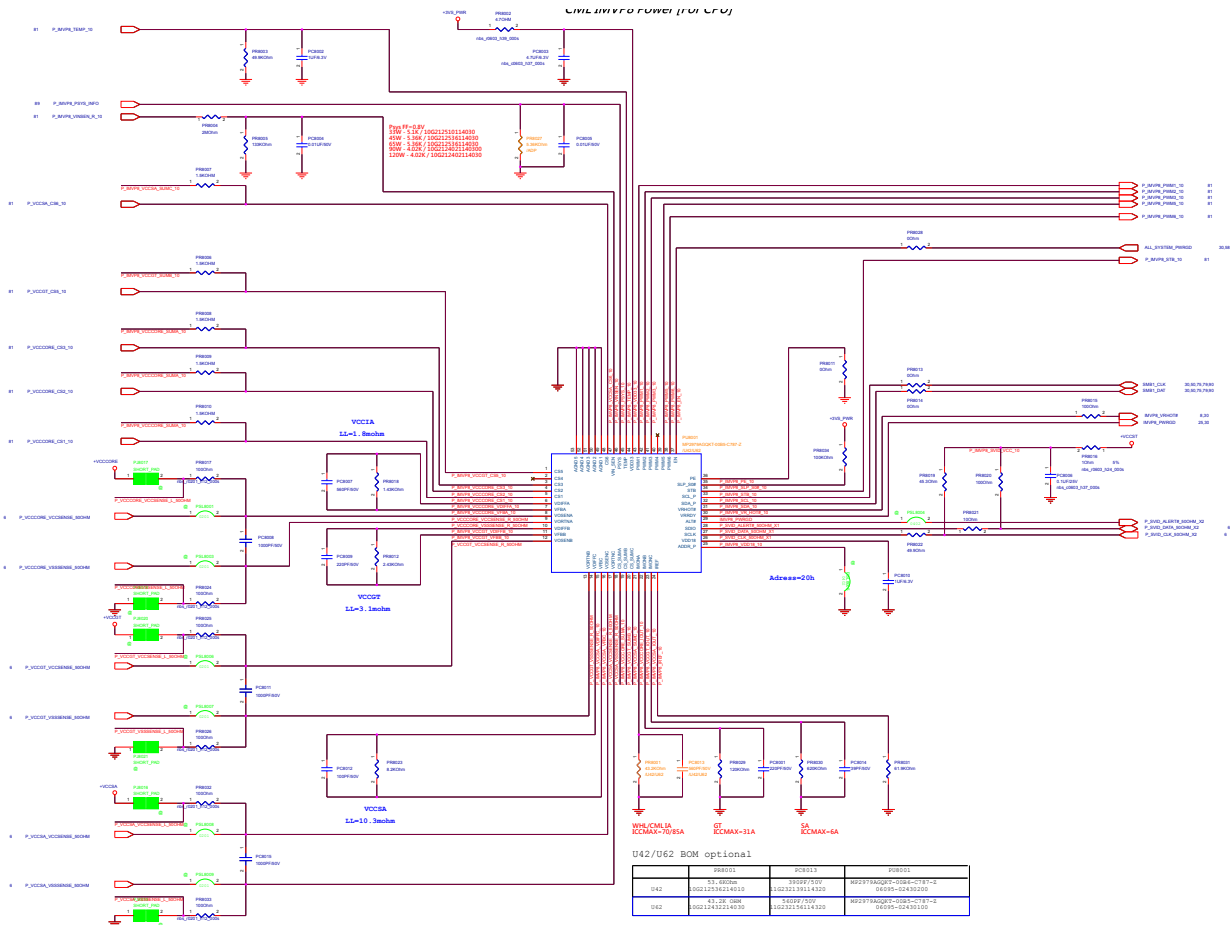


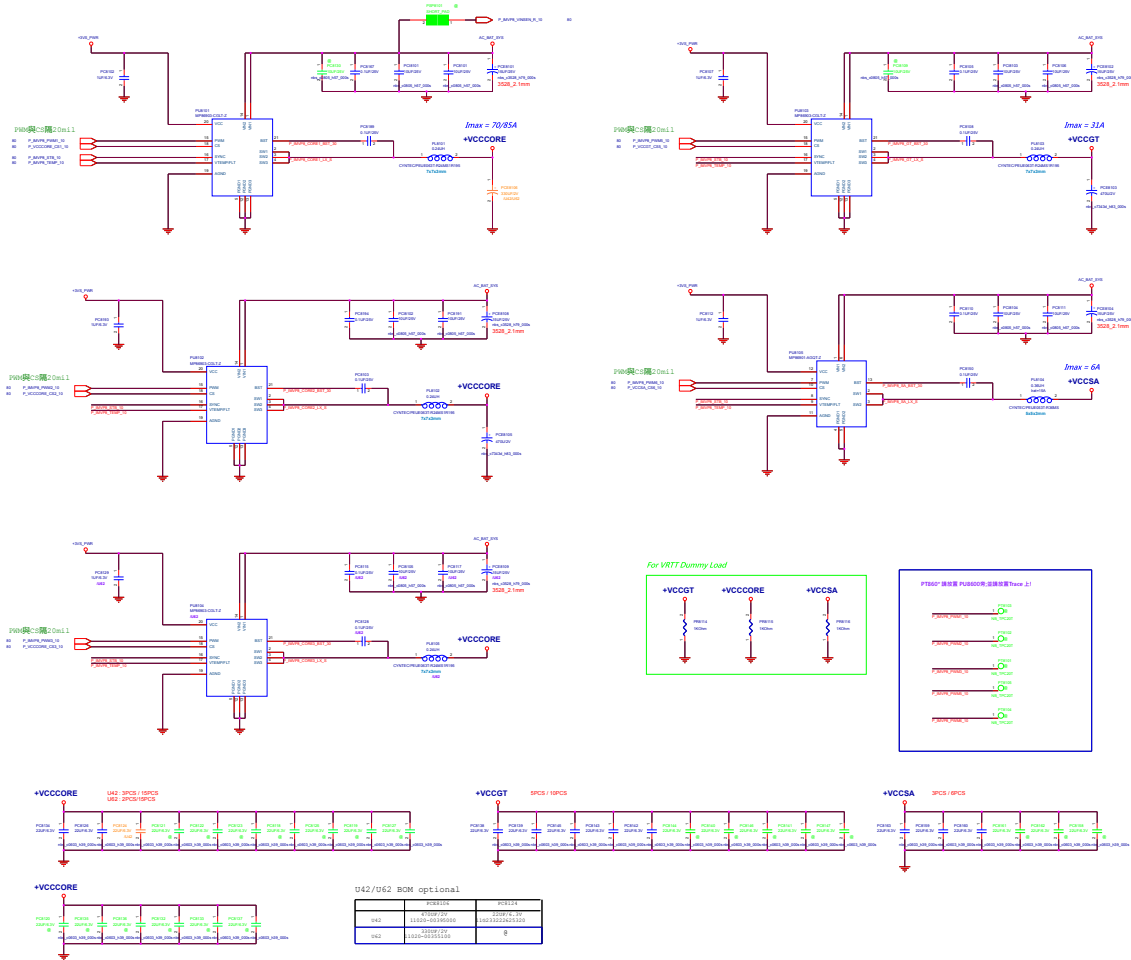
For Post time



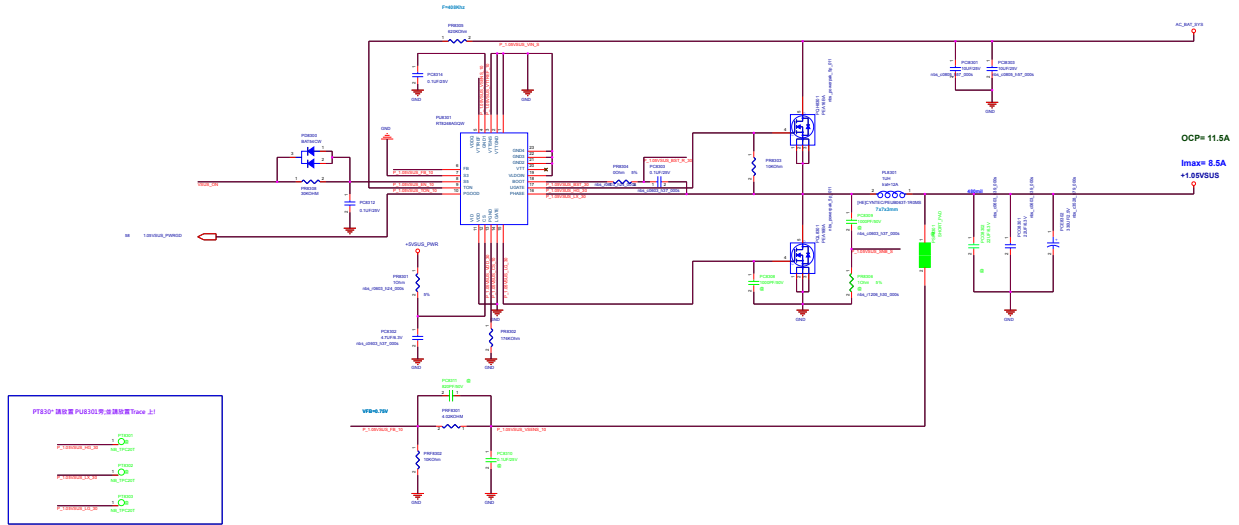
91 P_GPU_VRM_TEMP_SENSOR_10



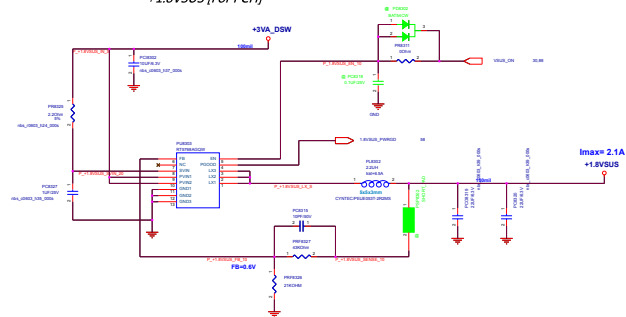




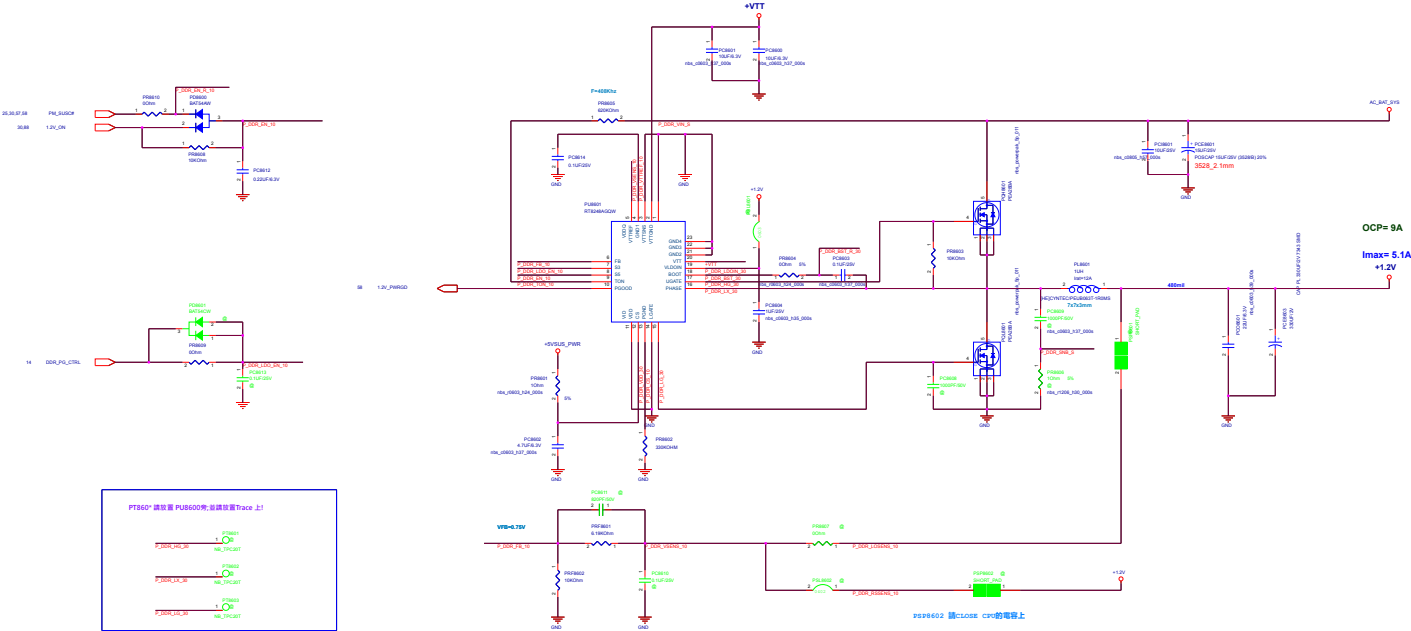
+1.05VSUS [For PCH]



+1.8VSUS [For PCH]

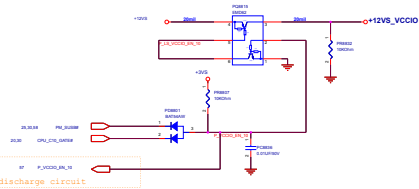
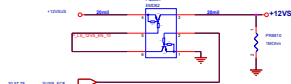
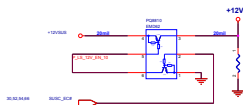
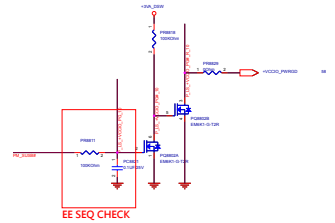
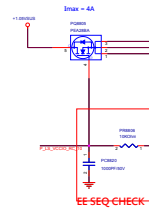
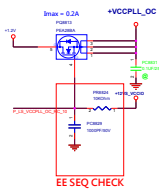
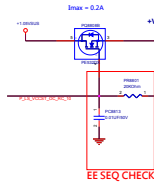
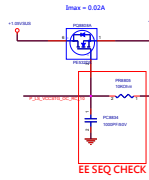
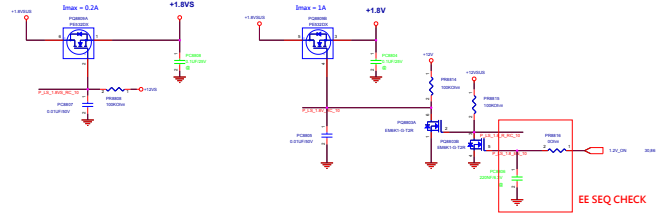
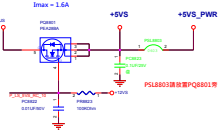
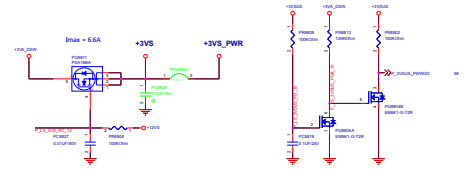
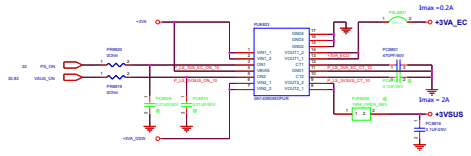


+1.2V / +VTT [For Memory]





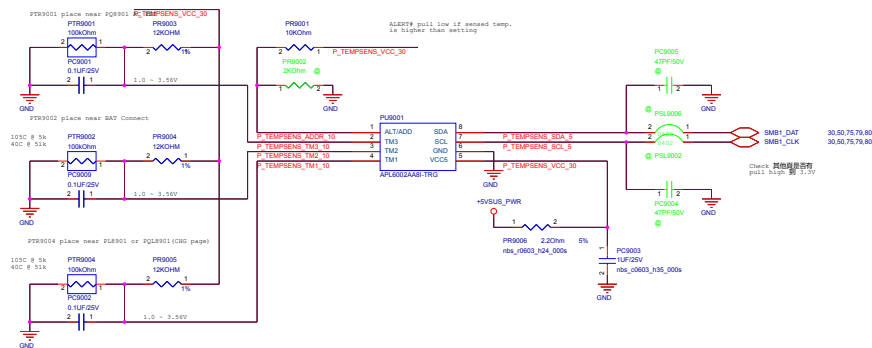
Load Switch



EE Add discharge circuit

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
FR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
FR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	Cx00	Cx01	Cx02	Cx03	Cx04	Cx05	Cx06
R/W	M	M	M	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



DC Jack Thermal Latch

P_LATCH_ACDB

PSL9005
SHORT LAND
1 4452 2

PQ9005B
EM1K1-G-T2R

GND

P_LATCH_OUT_10

PR9014
100KOhm

P_CHG_REGN_20

PR9017
10KOhm

P_CHG_REGN_20

PTR9003 place near DC JACK

PR9003
100KOhm

P_CHG_CMPIN_10

PC0008
0.1uF/25V

PR9022
7.52KOhm

P_CHG_CMPOUT_10

PR9016
10KOhm

P_CHG_ACCDET_10

PR9013
47.5KOhm



+NVVDD (For DGPU)

N17B Boost Voltage = 0.5V
N18B Boost Voltage = 0.5V

Part	Value	Unit
R1 (0.000001)	0.000001	Ω
R2 (0.000001)	0.000001	Ω
R3 (0.000001)	0.000001	Ω
R4 (0.000001)	0.000001	Ω
R5 (0.000001)	0.000001	Ω
R6 (0.000001)	0.000001	Ω
R7 (0.000001)	0.000001	Ω
R8 (0.000001)	0.000001	Ω
R9 (0.000001)	0.000001	Ω
R10 (0.000001)	0.000001	Ω
R11 (0.000001)	0.000001	Ω
R12 (0.000001)	0.000001	Ω
R13 (0.000001)	0.000001	Ω
R14 (0.000001)	0.000001	Ω
R15 (0.000001)	0.000001	Ω
R16 (0.000001)	0.000001	Ω
R17 (0.000001)	0.000001	Ω
R18 (0.000001)	0.000001	Ω
R19 (0.000001)	0.000001	Ω
R20 (0.000001)	0.000001	Ω
R21 (0.000001)	0.000001	Ω
R22 (0.000001)	0.000001	Ω
R23 (0.000001)	0.000001	Ω
R24 (0.000001)	0.000001	Ω
R25 (0.000001)	0.000001	Ω
R26 (0.000001)	0.000001	Ω
R27 (0.000001)	0.000001	Ω
R28 (0.000001)	0.000001	Ω
R29 (0.000001)	0.000001	Ω
R30 (0.000001)	0.000001	Ω
R31 (0.000001)	0.000001	Ω
R32 (0.000001)	0.000001	Ω
R33 (0.000001)	0.000001	Ω
R34 (0.000001)	0.000001	Ω
R35 (0.000001)	0.000001	Ω
R36 (0.000001)	0.000001	Ω
R37 (0.000001)	0.000001	Ω
R38 (0.000001)	0.000001	Ω
R39 (0.000001)	0.000001	Ω
R40 (0.000001)	0.000001	Ω
R41 (0.000001)	0.000001	Ω
R42 (0.000001)	0.000001	Ω
R43 (0.000001)	0.000001	Ω
R44 (0.000001)	0.000001	Ω
R45 (0.000001)	0.000001	Ω
R46 (0.000001)	0.000001	Ω
R47 (0.000001)	0.000001	Ω
R48 (0.000001)	0.000001	Ω
R49 (0.000001)	0.000001	Ω
R50 (0.000001)	0.000001	Ω
R51 (0.000001)	0.000001	Ω
R52 (0.000001)	0.000001	Ω
R53 (0.000001)	0.000001	Ω
R54 (0.000001)	0.000001	Ω
R55 (0.000001)	0.000001	Ω
R56 (0.000001)	0.000001	Ω
R57 (0.000001)	0.000001	Ω
R58 (0.000001)	0.000001	Ω
R59 (0.000001)	0.000001	Ω
R60 (0.000001)	0.000001	Ω
R61 (0.000001)	0.000001	Ω
R62 (0.000001)	0.000001	Ω
R63 (0.000001)	0.000001	Ω
R64 (0.000001)	0.000001	Ω
R65 (0.000001)	0.000001	Ω
R66 (0.000001)	0.000001	Ω
R67 (0.000001)	0.000001	Ω
R68 (0.000001)	0.000001	Ω
R69 (0.000001)	0.000001	Ω
R70 (0.000001)	0.000001	Ω
R71 (0.000001)	0.000001	Ω
R72 (0.000001)	0.000001	Ω
R73 (0.000001)	0.000001	Ω
R74 (0.000001)	0.000001	Ω
R75 (0.000001)	0.000001	Ω
R76 (0.000001)	0.000001	Ω
R77 (0.000001)	0.000001	Ω
R78 (0.000001)	0.000001	Ω
R79 (0.000001)	0.000001	Ω
R80 (0.000001)	0.000001	Ω
R81 (0.000001)	0.000001	Ω
R82 (0.000001)	0.000001	Ω
R83 (0.000001)	0.000001	Ω
R84 (0.000001)	0.000001	Ω
R85 (0.000001)	0.000001	Ω
R86 (0.000001)	0.000001	Ω
R87 (0.000001)	0.000001	Ω
R88 (0.000001)	0.000001	Ω
R89 (0.000001)	0.000001	Ω
R90 (0.000001)	0.000001	Ω
R91 (0.000001)	0.000001	Ω
R92 (0.000001)	0.000001	Ω
R93 (0.000001)	0.000001	Ω
R94 (0.000001)	0.000001	Ω
R95 (0.000001)	0.000001	Ω
R96 (0.000001)	0.000001	Ω
R97 (0.000001)	0.000001	Ω
R98 (0.000001)	0.000001	Ω
R99 (0.000001)	0.000001	Ω
R100 (0.000001)	0.000001	Ω

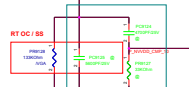
12PM FUNCTION

SPIN FUNCTION

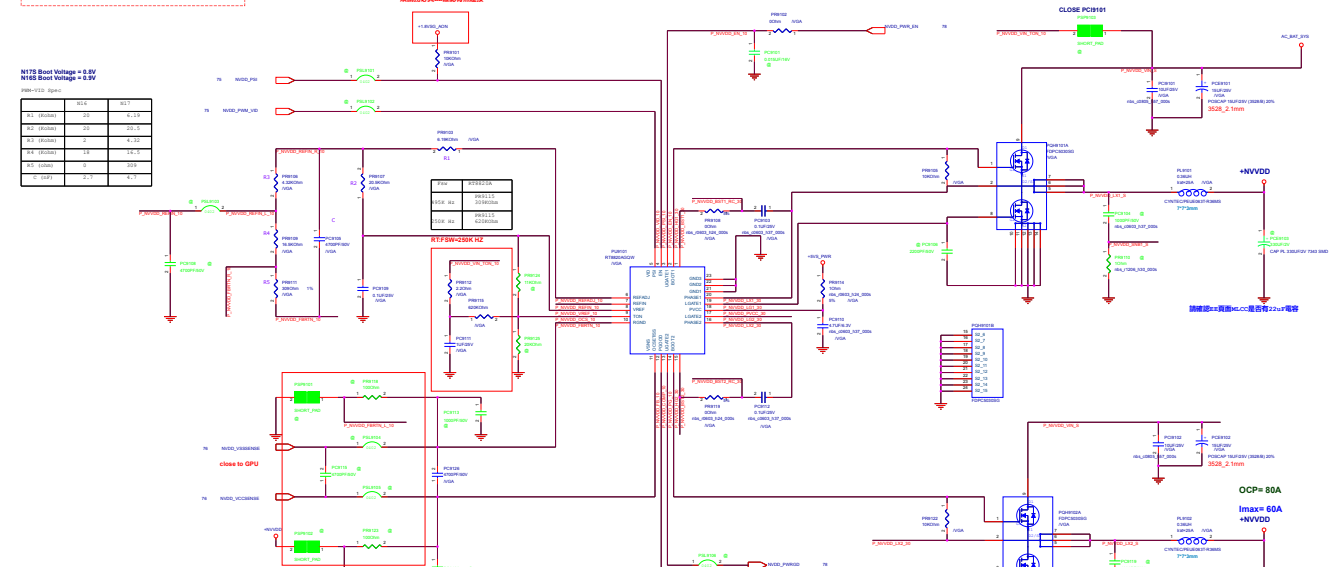
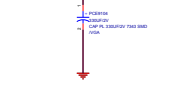
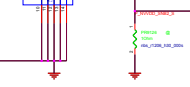
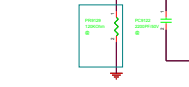
OC-LAY	OC-150A	OC-150B	OC-150C
OC-150A	0	0	0
OC-150B	0	0	0
OC-150C	0	0	0
OC-150D	0	0	0
OC-150E	0	0	0
OC-150F	0	0	0
OC-150G	0	0	0
OC-150H	0	0	0
OC-150I	0	0	0
OC-150J	0	0	0
OC-150K	0	0	0
OC-150L	0	0	0
OC-150M	0	0	0
OC-150N	0	0	0
OC-150O	0	0	0
OC-150P	0	0	0
OC-150Q	0	0	0
OC-150R	0	0	0
OC-150S	0	0	0
OC-150T	0	0	0
OC-150U	0	0	0
OC-150V	0	0	0
OC-150W	0	0	0
OC-150X	0	0	0
OC-150Y	0	0	0
OC-150Z	0	0	0

OC-LAY	OC-150A	OC-150B	OC-150C
OC-150A	0	0	0
OC-150B	0	0	0
OC-150C	0	0	0
OC-150D	0	0	0
OC-150E	0	0	0
OC-150F	0	0	0
OC-150G	0	0	0
OC-150H	0	0	0
OC-150I	0	0	0
OC-150J	0	0	0
OC-150K	0	0	0
OC-150L	0	0	0
OC-150M	0	0	0
OC-150N	0	0	0
OC-150O	0	0	0
OC-150P	0	0	0
OC-150Q	0	0	0
OC-150R	0	0	0
OC-150S	0	0	0
OC-150T	0	0	0
OC-150U	0	0	0
OC-150V	0	0	0
OC-150W	0	0	0
OC-150X	0	0	0
OC-150Y	0	0	0
OC-150Z	0	0	0

RT OC / SS
ROCHvalley/Val12/18uA
RT OCL48A



OC-150E/2 Row# 2.0+1.1m
L=0.22u; H=2500Hz; dh=15.8A
L=0.38u; H=2500Hz; dh=4.6A



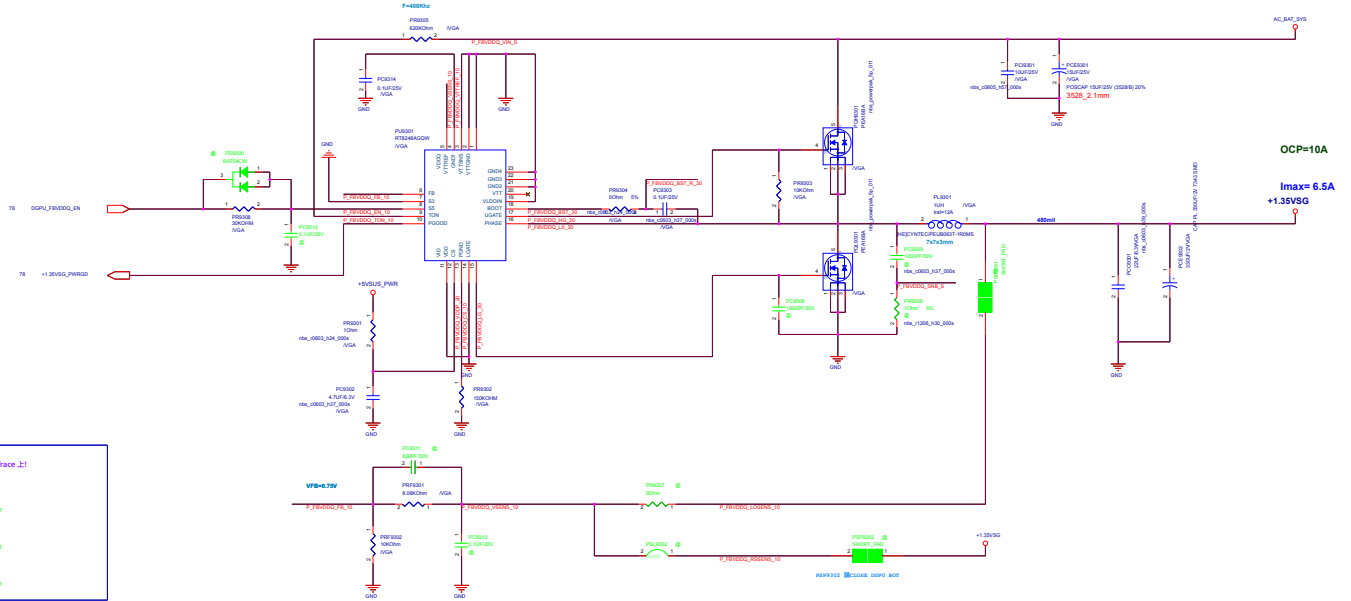
OC-150E/2 Row# 2.0+1.1m
L=0.22u; H=2500Hz; dh=15.8A
L=0.38u; H=2500Hz; dh=4.6A

OC-150E/2 Row# 2.0+1.1m
L=0.22u; H=2500Hz; dh=15.8A
L=0.38u; H=2500Hz; dh=4.6A

OC-150E/2 Row# 2.0+1.1m
L=0.22u; H=2500Hz; dh=15.8A
L=0.38u; H=2500Hz; dh=4.6A

OC-150E/2 Row# 2.0+1.1m
L=0.22u; H=2500Hz; dh=15.8A
L=0.38u; H=2500Hz; dh=4.6A

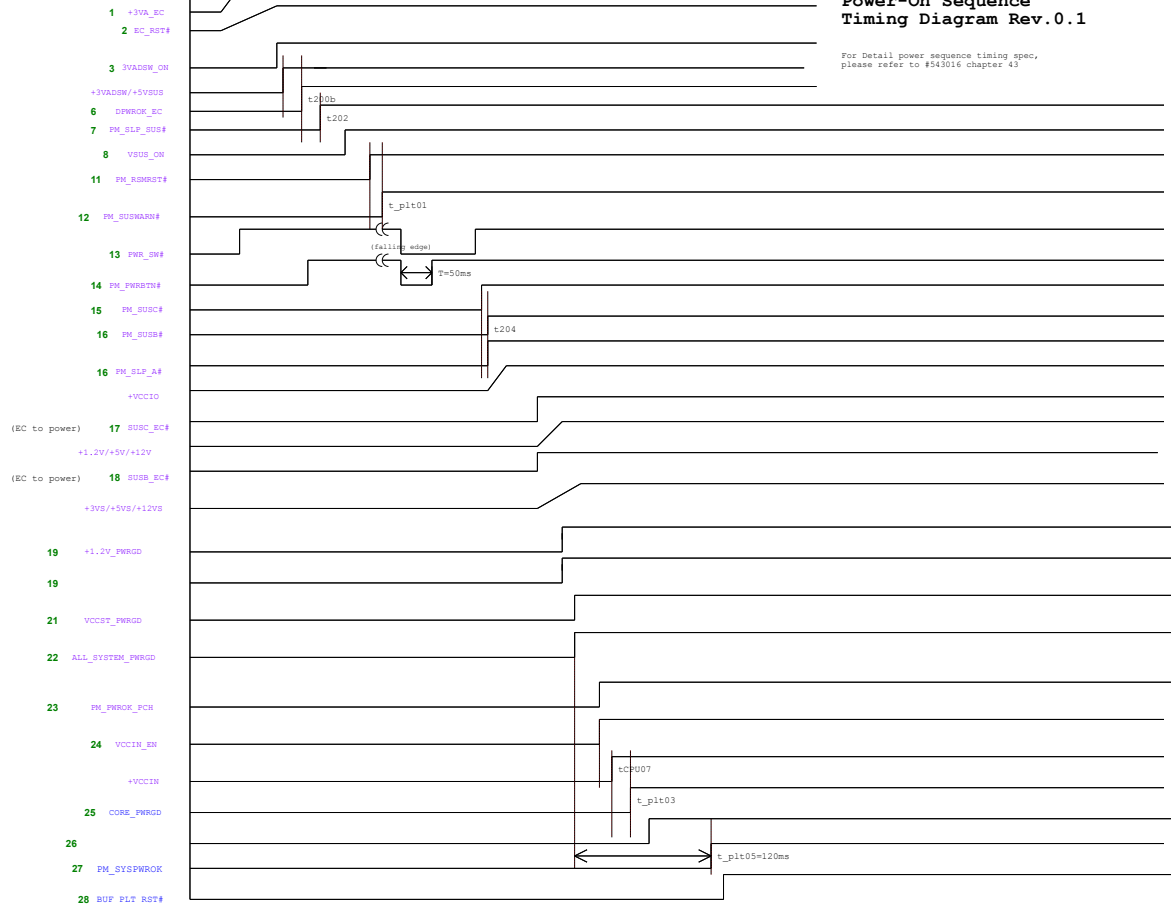
+FBVDDQ [For VRAM]



PT930* 請放置 PU9301 旁邊請放置Trace上!

PJ.FBVDQD_VDDQ_W
PUB001
PUB002
PUB003
PUB004

AC-IN Mode



AC-IN Mode

Power On Sequence Diagram Rev.2.0

